United Monolithic Semiconductors

CHA3801-FAB

L-Band Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

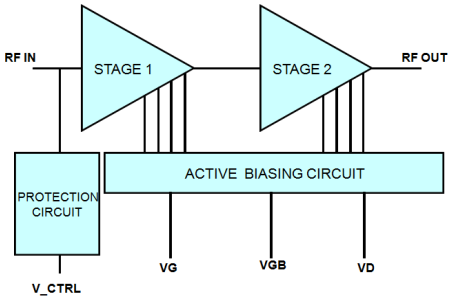
Description

The CHA3801-FAB is an L-Band LNA monolithic circuit including an active bias network. In addition, a protection network is included to allow high input power survivability.

It is designed for a wide range of applications, from space, military to commercial communication systems.

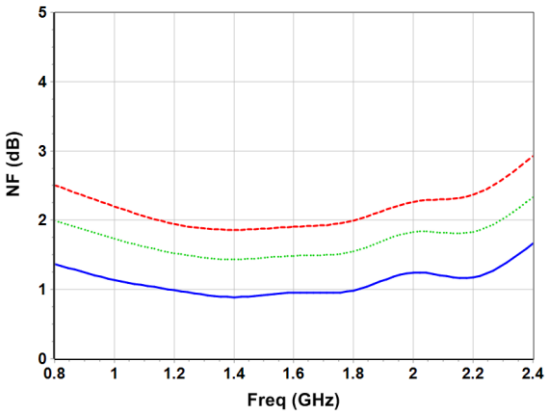
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- L-Band performances: 1-2GHz
- 1.5dB Noise Figure
- 28dB Linear Gain
- 17dBm Saturated Output Power
- 27dBm Output Third Order Intercept
- DC bias: Vd = 5Volt @ 70mA
- 6x6mm² hermetic metal ceramic package
- MSL3



Typical Noise Figure versus Temperature

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1		2	GHz
Gain	Linear Gain		28		dB
NF	Noise Figure		1.5		dB
Pout	Output Power @1dB comp.		16		dBm

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Operating Modes

Mode	Description	Pin #2	Pin #3	Pin #20	Pin #4
1a	Nominal bias current	-5V	n.c.*	-5V	+5V
1b	High bias current	n.c.*	-5V	-5V	+5V
1c	Low bias current	-5V	-5V	-5V	+5V

* Not connected

Input protection state	Pin #20			
enabled	GND			
disabled	-5V			

Electrical Characteristics

Tamb.= +25°C, Vd = +5V under working mode 1a and input protection disabled

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1		2	GHz
Gain	Gain		28		dB
-	Gain flatness		1		dBp-p
Rlin	Input Return Loss		-15		dB
Rlout	Output Return Loss		-15		dB
NF	Noise Figure		1.5		dB
|S12|	Reverse Isolation		45		dB
OP1dB	Output 1 dB Compression Point		16		dBm
Id_1a	Total drain Current (mode 1a)		75		mA
Id_1b	Total drain Current (mode 1b)		100		mA
Id_1c	Total drain Current (mode 1c)		50		mA
Vd	Drain Voltage		5		V
Vg	Gate Voltage		-5		V
Tj	Junction temperature			175	°C

These values are representative of measurements on board

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage (Vg=-5V)	6.5	V
Vctrl	Control voltage	-6 to 0	V
Vg	Gate bias voltage (Vd=+5V)	-6 to 0	V
Pin	Protection switch enabled	+17	dBm
Pin	Protection switch disabled	+6	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pin N°	Parameter	Values	Unit
VD	4	Drain voltage	+5	V
VG	2	Gate voltage	–5 / 0	V
VGB	4	Gate voltage	-5 / 0	V
C	2	Input protection control	–5 / 0	V

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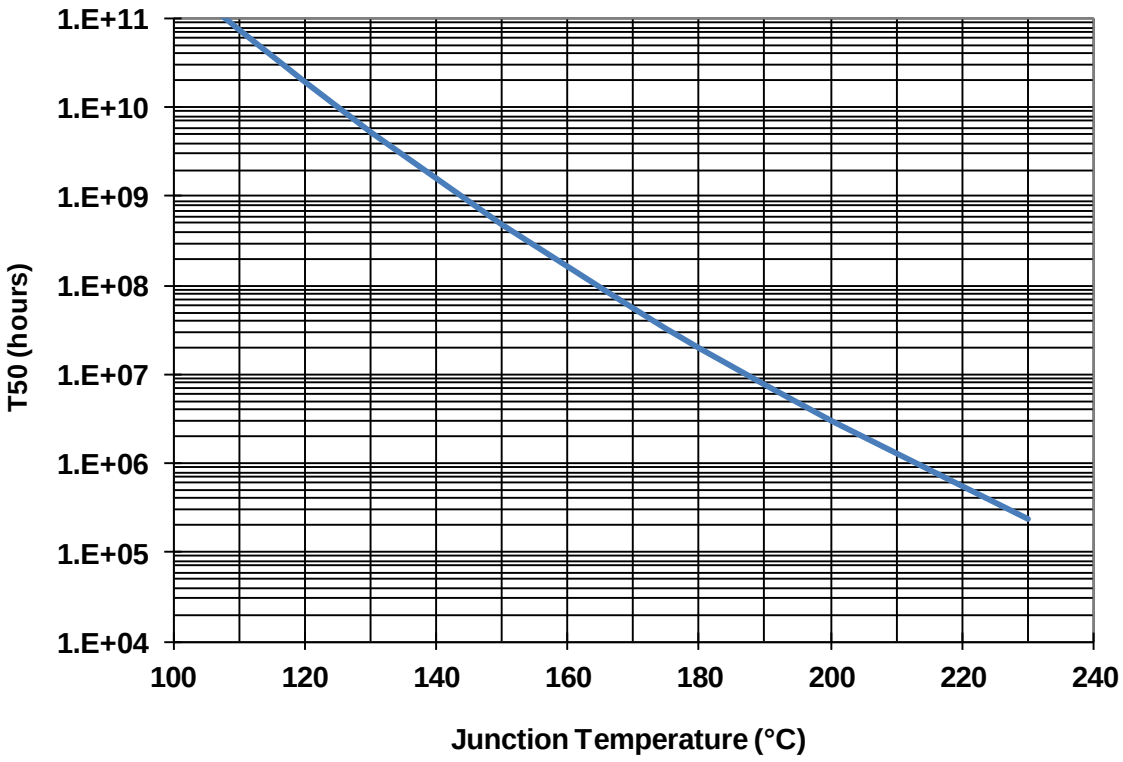
Device thermal performances

All the figures given in this section are obtained assuming that the packaged device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
Consequently, your system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd = 5V Idq = 70mA(2) Pdiss = 0.35W	122	105	2E+10

(1) Assuming 85°C Tcase
(2) Idq at 85°C Tcase when Vg set to get Idq = 75mA at 25°C Tcase



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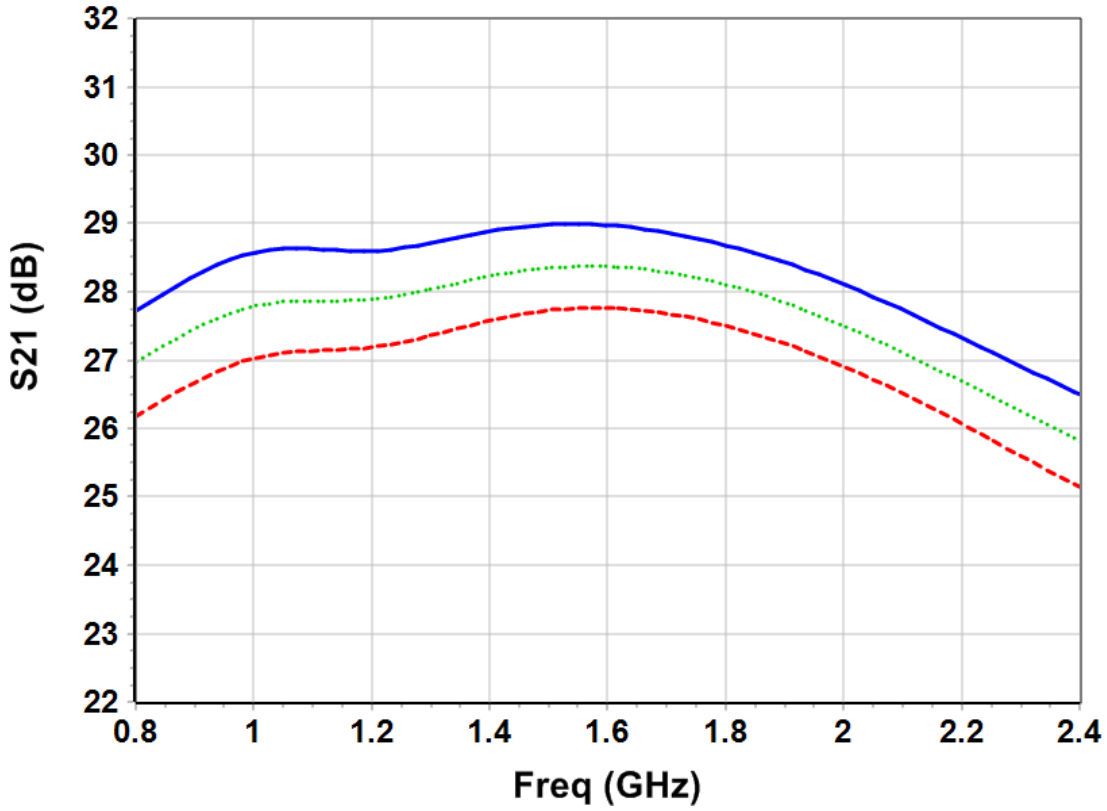
Typical Board Measurements

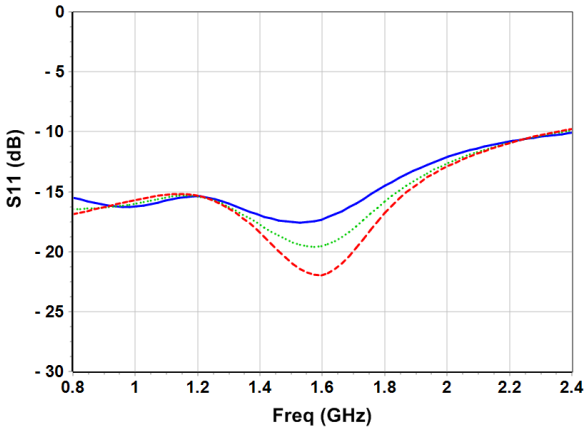
Temperature -40°C, +25°C, +85°C
Vd = +5V, working mode 1a with input protection disabled

Linear Gain versus Frequency

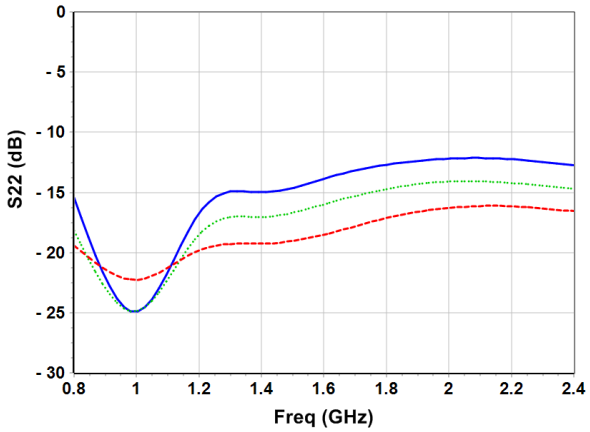


— -40°C . . . +25°C - - -+85°C

Input Return Loss versus Frequency



Output Return Loss versus Frequency



— -40°C . . . +25°C - - -+85°C

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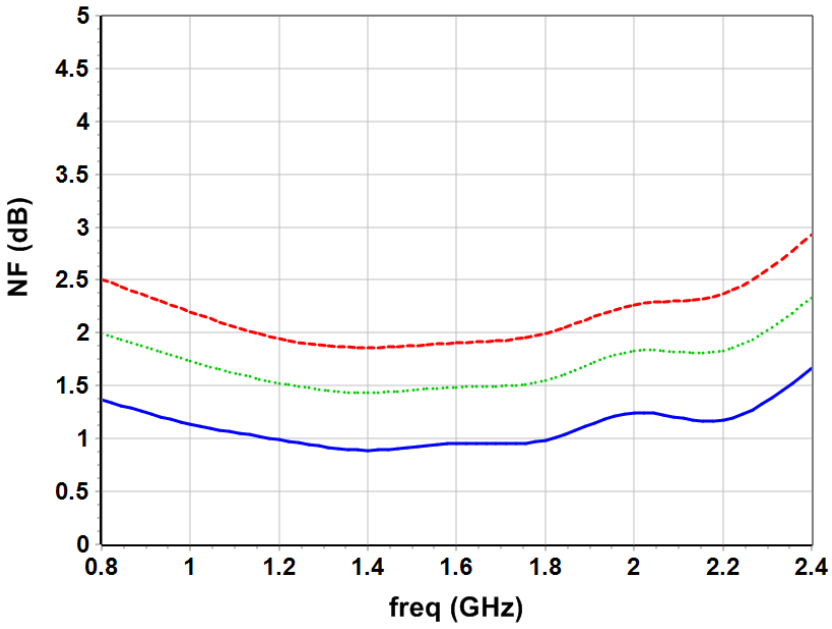
Typical Board Measurements

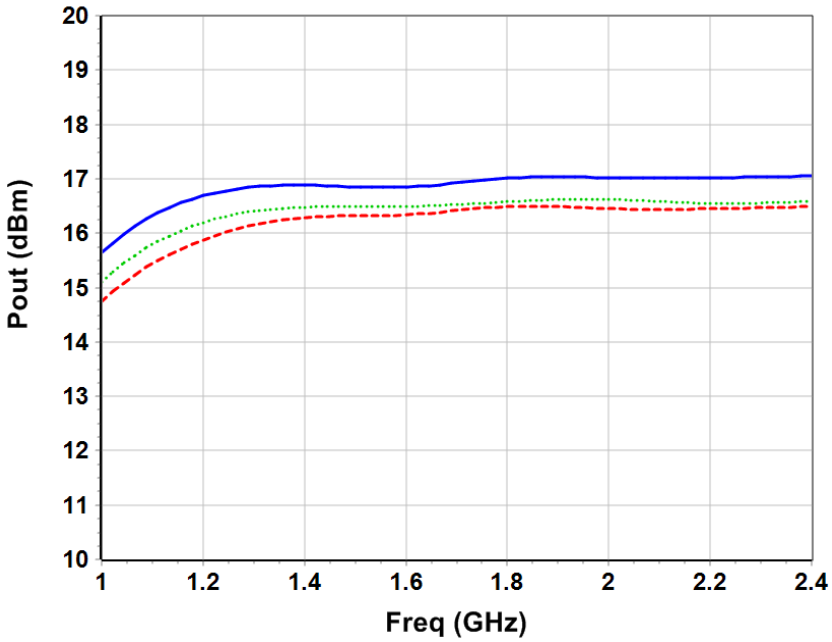
Temperature -40°C, +25°C, +85°C
Vd = +5V, working mode 1a with input protection disabled

Noise Figure versus Frequency



— -40°C - - - - +25°C — - +85°C

Output power @ 1dB comp. versus Frequency



— -40°C - - - - +25°C — - +85°C

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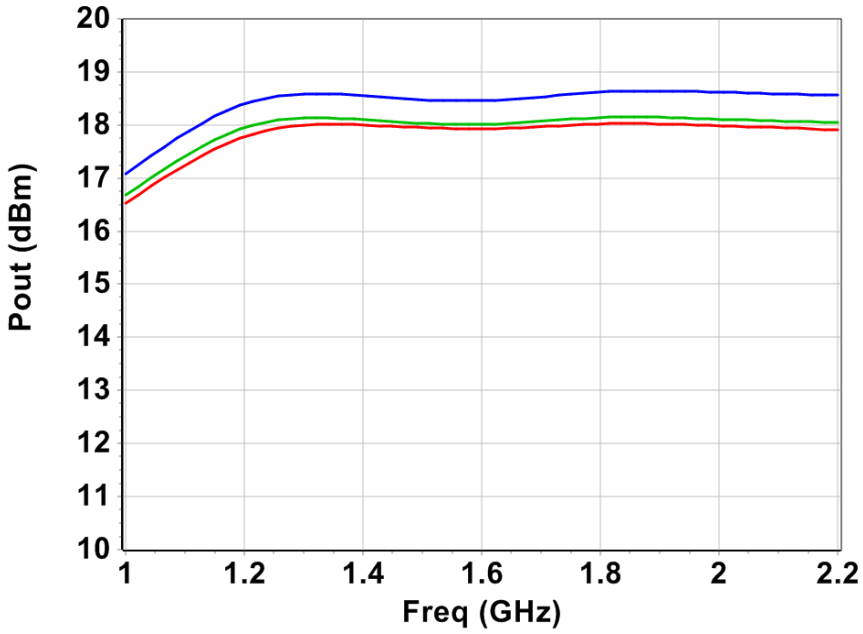
Typical Board Measurements

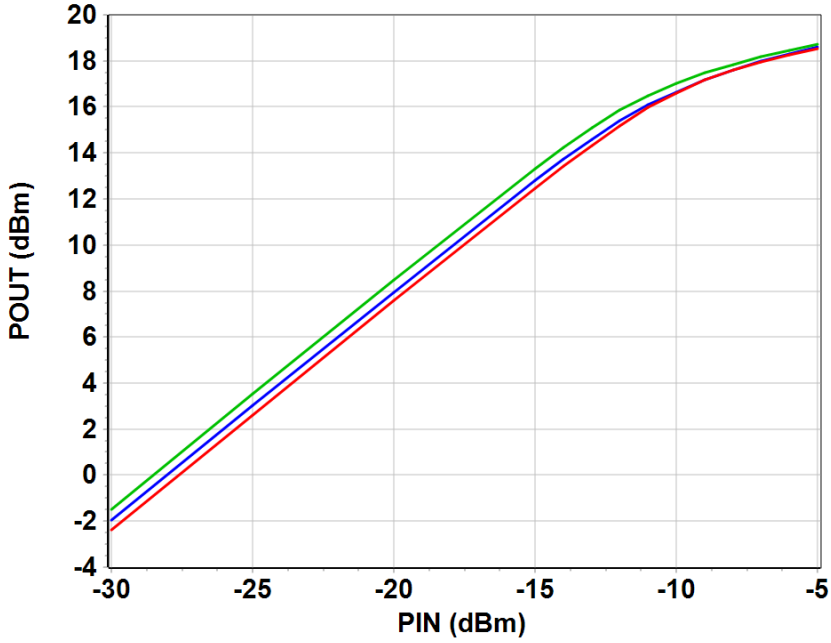
Temperature -40°C, +25°C, +85°C
Vd = +5V, working mode 1a with input protection disabled

Output power @ Sat versus Frequency



-40°C **+25°C** **+85°C**

Output power versus Input Power @ 25°C



1.2GHz **1.6GHz** **2GHz**

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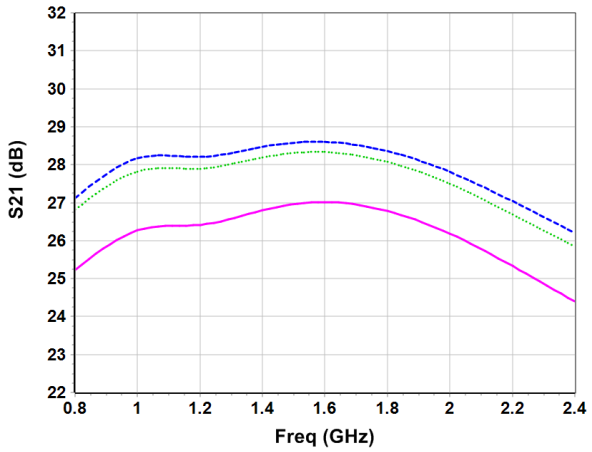
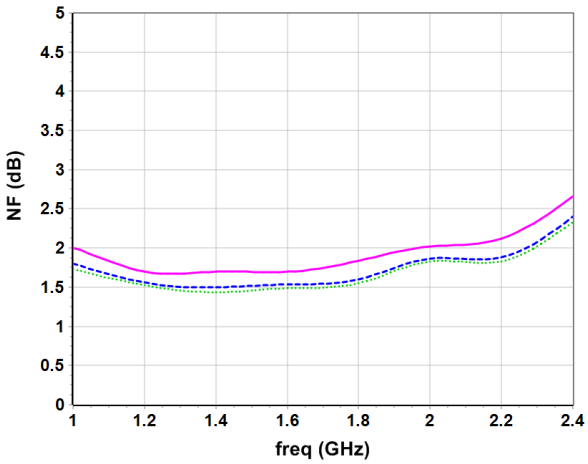
Typical Board Measurements

Tamb.= +25°C, Vd = +5V, working with input protection disabled

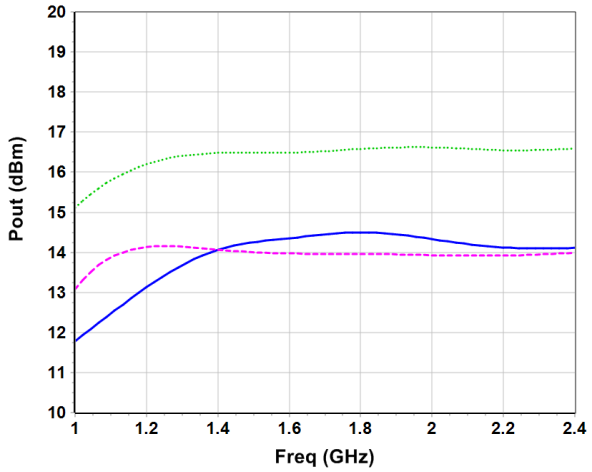
Linear gain



Noise Figure versus Frequency



Output power @ 1dB comp. versus Frequency



— Mode 1c - - - - Mode 1a — - Mode 1b

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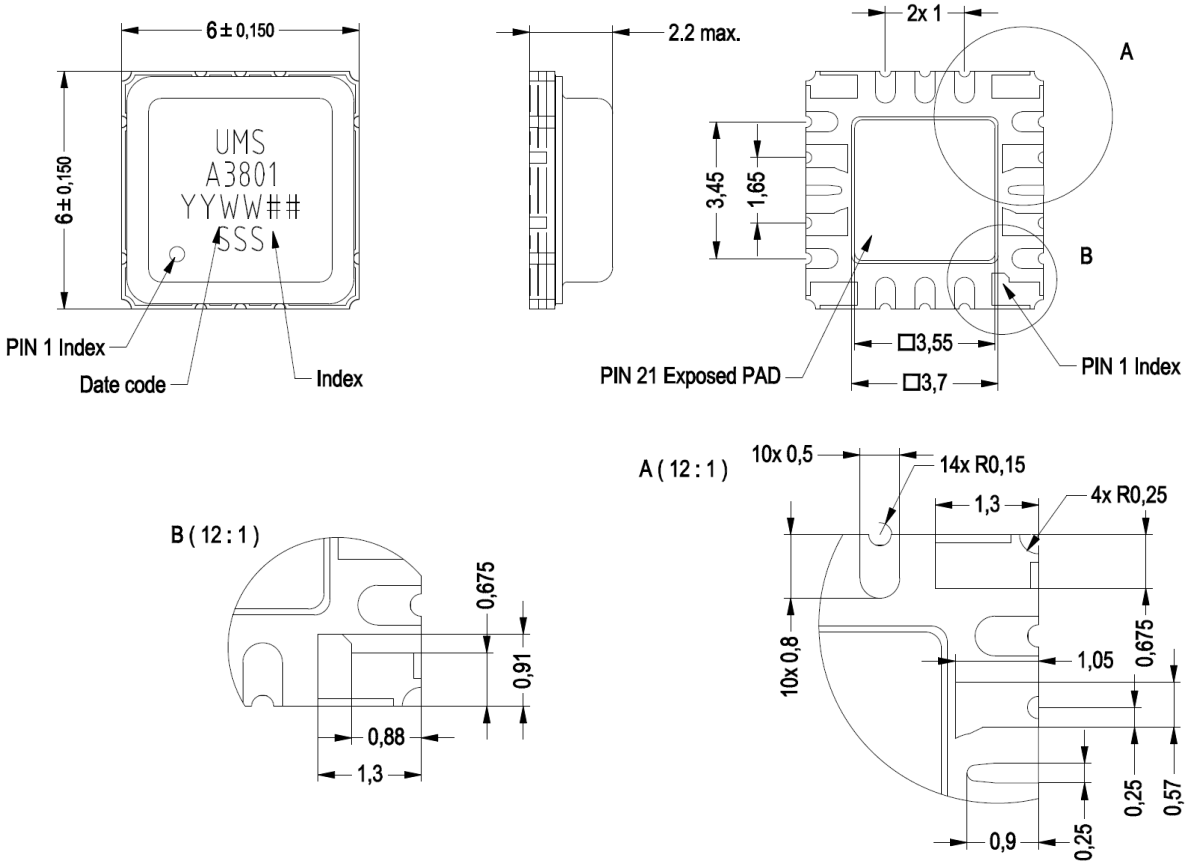
Package outline



1- GND	8- RF OUT	15- GND
2- VG	9- GND	16- Nc
3- VGB	10- Nc	17- GND
4- VD	11- GND	18- RF IN
5- GND	12- Nc	19- GND
6- Nc	13- Nc	20- C
7- GND	14- Nc	21- GND

Dimensions in mm

(1) The package outline drawing included in this data-sheet is given for indication. Refer to the application note AN0024 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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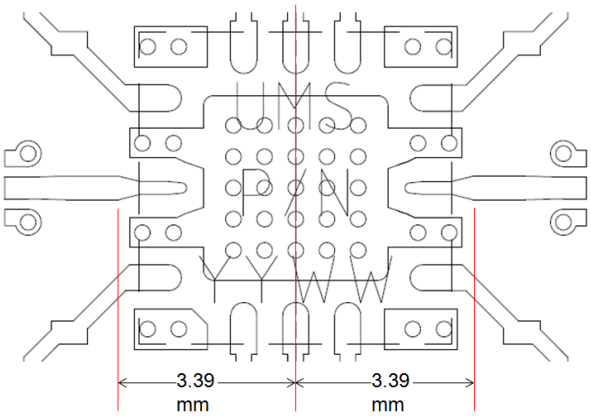
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.39mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Package Information

Parameter	Value
Package body material	RoHS-compliant
Lead finish	Gold
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	$1x10^{-8}$ ccHe/s/atm

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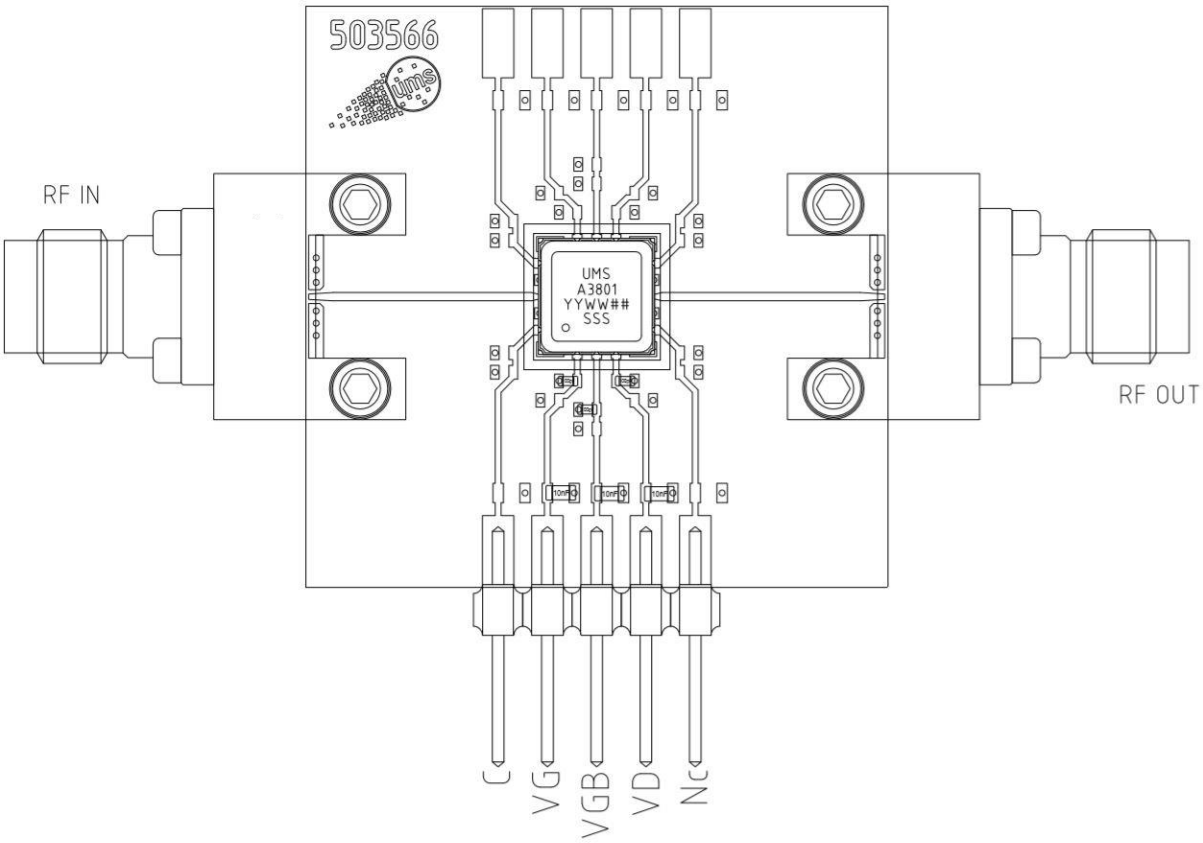
Evaluation board description

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF are recommended on each DC access (C / VG / VGB / VD)



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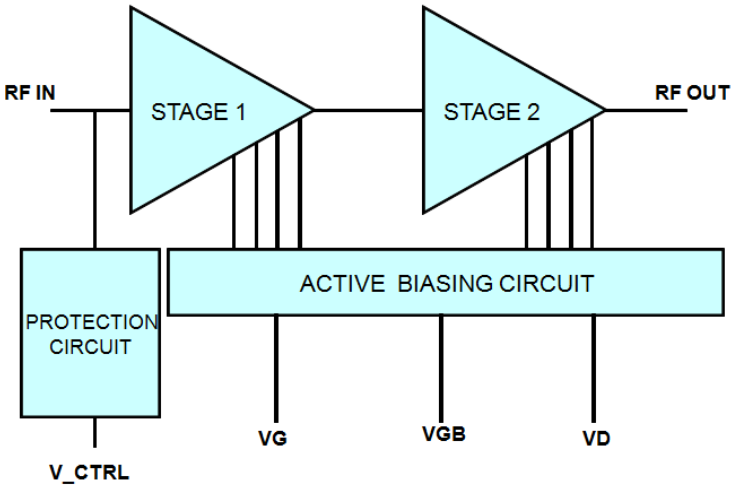
Block Diagram

Block diagram of the LNA



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SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

FAB Type Surface Mount Hermetic Package

Refer to the application note AN0024 available at https://www.ums-rf.com for assembly recommendations for the UMS FAB package products.

Ordering Information

Leadless hermetic package:	CHA3801-FAB/XY Waffle pack: XY = 24

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