United Monolithic Semiconductors

AN0025

Application Note:

Influence of the thermal measurement methodology on thermal resistance estimation for III-V device

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SUMMARY

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[1] "Thermal and trapping phenomena assessment on AlGaN/GaN microwave power transistor", G. Mouginot et al. *Proceedings of the 5th European Microwave Integrated Circuits Conference, 27-28 September 2010, Paris, France. p. 110-113*

[2] "Combined Infrared and Raman temperature measurements on device structures", A. Sarua et al. *CS MANTECH Conference, April 24-27, 2006, Vancouver, British Columbia, Canada, p 179-182*

[3] "Comprehensive Thermal Analysis of Pulsed GaAs HPAs for Lifetime Estimation", J. W. Pomeroy et al. *IMS Montreal (2012)*

[4] "Temperature Assessment of AlGaN/GaN HEMTs: A Comparative study by Raman, Electrical and IR Thermography", N. Killat & M. Kuball. *IRPS (2010)*

[5] "Thermal Boundary Resistance Between GaN and Substrate in AlGaN/GaN Electronic Devices", A. Sarua et al. *IEEE Transctions On Electron Devices, Vol. 54, No. 12, December 2007*

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1. Introduction

This application note aims to provide a guideline on how to use thermal data mentioned in UMS product datasheets to evaluate the reliability of the product in a given environment.

An overview of the definition of the junction temperature and of the thermal resistance is also given. The impact of the measurement method on the junction temperature evaluation and the associated thermal resistance is illustrated for GaAs and GaN devices.

2. UMS methodology for T_j evaluation and R_{th} calculation

The junction temperature mentioned in UMS datasheets corresponds to the “simulated maximum peak junction temperature”. The thermal resistance is calculated using this value and determined through two different ways depending whether the device is a chip or a packaged product.

2.1 Chip case

For a circuit in die form, the junction temperature is evaluated from a thermal model via 3D thermal simulation software, either directly, or based on a set of equations fitted against such simulation results.

The thermal model is calibrated by an intensive preliminary work to estimate the physical parameters of each layer (thermal conductivity and specific heat) and interface (thermal contact resistance) in between layers [5]. These parameters have been previously tuned thanks to accurate thermal measurement based on different techniques presented in the following.

Then using 2D physics-based simulation, it is possible to determine the exact dimensions of the heat source to inject the total dissipated power in the device.

Thanks to this approach, a very good estimation of the “maximum peak junction temperature” is obtained.

The equivalent thermal resistance R_{th_chip} of the device is given by:

$$R_{th\_chip} = \frac{T_j - T_b}{P_{diss\_tot}} \qquad \textit{Eq.1}$$

Where T_j is the simulated maximum peak junction temperature obtained on the hottest transistor, T_b is the backside temperature of the chip (substrate), and P_{diss_tot} is the total dissipated power in the device.

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2.2 Packaged product Case

The thermal resistance of a packaged device can be represented as the sum of the contributors as shown in the figure below:

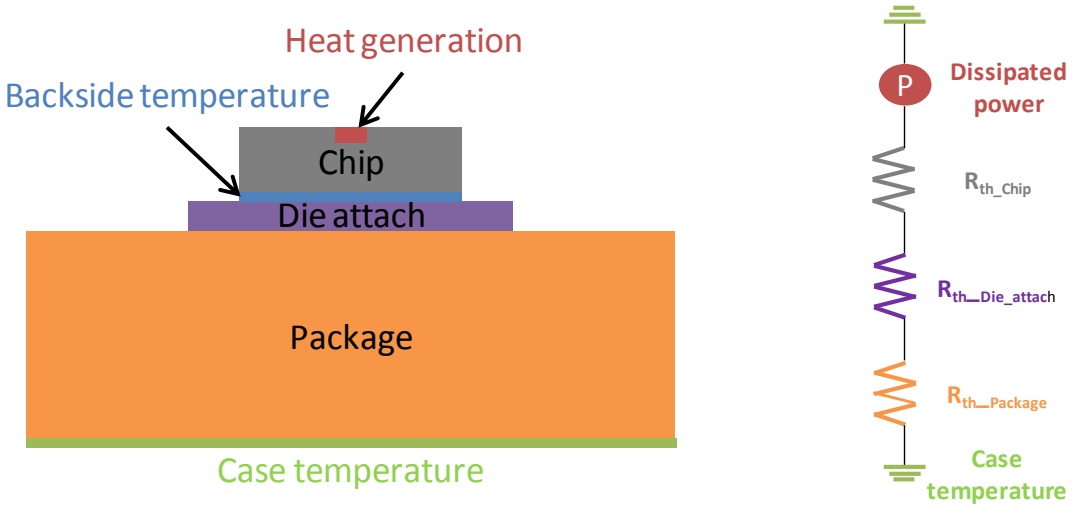

Fig. 1: Schematic cross section of a packaged device (left) and thermal model (right)

For a packaged product, the junction temperature is determined through the use of simulations and/or characterizations. Indeed, the thermal coupling between the elementary transistors has an impact on overall thermal resistance which depends on the layout of the chip (relative position of the transistors) and on the thermal properties of the package.

The junction temperature of the hottest transistor is estimated using the thermal resistance value of the chip (R_{th_chip}) and the thermal resistance of the assembly. This calculation has to be done for a given package backside temperature and a given dissipated power.

The equivalent thermal resistance $R_{th\_packaged\_product}$ of the packaged MMIC is expressed as:

$$R_{th\_packaged\_product} = \frac{T_j - T_c}{P_{diss\_tot}} \qquad \text{Eq.2}$$

Where T_j is the junction temperature of the hottest transistor of the MMIC, T_c is the backside temperature of the package, and P_{diss_tot} is the total dissipated power in the MMIC.

Note the thermal resistance given in UMS data sheet is noted R_{th_eq} and corresponds either to R_{th_chip} or $R_{th\_packaged\_product}$ depending whether the device is a chip or a packaged product.

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2.3 Relationship between the R_{th} and the T_{50}

A direct correlation exists in between the thermal resistance (R_{th}) and the median time to failure (T_{50}) derived from process qualification.

The temperature of the devices in the reliability tests is defined from the methodology explained in this document. It means that the maximum peak junction temperature (T_j) is used as a reference to extract the value of the thermal resistance (R_{th}) of the test vehicle used during the qualification of the process. This is recognized as the more realistic statement from a reliability analysis.

The Arrhenius plot given in the next figure and showing the evolution of T_{50} as a function of *Tj* takes into account this approach through the temperature calculation on the x-axis.

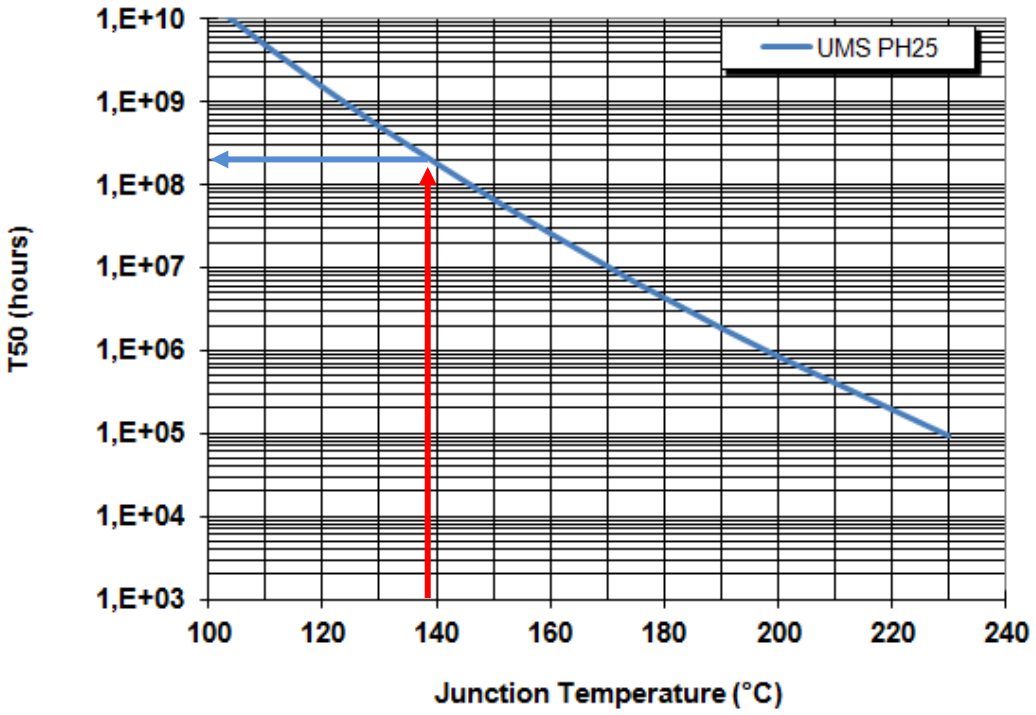

Figure 2: Example T_{50} versus maximum peak junction temperature (Tj) from the PH25 process. It is based on the hot spot approach Rth calculation.

2.4 Example – Extract from the CHA3666-99F data-sheet (PH25 process)

The temperature T_b is defined as the chip backside temperature. The equivalent thermal resistance (R_{th_eq}) is given for the full circuit, and assumes CW mode operation by default.

Parameter	Symbol	Conditions	Values	Unit
Thermal Resistance	R_{th_eq}	T_b = 85 °C, 4 V, 80 mA (P_{diss_tot} = 0.32 W)	169	°C/W
Junction Temperature	T_j		139	°C
Median Lifetime	T_{50}		2.0×10^8	Hrs

Table 1: Example for a typical UMS product (CHA3666-99F)

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3. Junction temperature estimation techniques

There are several methods and techniques to estimate the temperature of electronic devices under operating conditions. [1] [2] [3] [4]

3.1 Electrical method

This approach is based on the temperature dependency of some sensitive electrical parameters of the transistors such as R_{on} and I_{DS}. It consists in pulsed I-V measurement versus temperature at zero power dissipation and at a fixed temperature for different levels of dissipated power. Note this method gives an average temperature of the active area of the device.

3.2 IR microscopy

This method is based on radiation heat transfer. It presents a spatial resolution down to 2 µm and allows performing large temperature mapping of the surface of the device in DC, or localized area mapping in transient. The temperature is averaged over a spot of 2 - 3 µm diameters on the surface of the device. Note this technique cannot be used on metallic elements.

3.3 Micro-Raman microscopy

This approach is based on phonon scattering spectroscopy. It presents a spatial resolution down to 0.5 µm and allows measuring the temperature in depth into the volume of the device. The temperature is spatially averaged over a 1 µm diameter spot in the volume of the GaN or GaAs layer.

3.4 Thermoreflectance thermography

This approach is based on the temperature dependency of material reflectivity. It presents a spatial resolution of 1 µm and allows performing transient temperature mapping of the surface of the device. The temperature is averaged on metallic surface over a 1 µm diameter spot.

3.5 3D thermal simulation

3D thermal numerical simulation is based on a finite element method. This one allows determining the temperature accurately in the active area of the device under operating conditions. This approach needs to be calibrated by one or several experimental temperature estimation techniques.

The junction temperature is extracted down to a nanometer scale in the active area of the device. This one is called the “simulated maximum peak junction temperature” and referenced as *Tj* in this document. This last method is also called the “hot spot” method.

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3.6 Synthesis

As a conclusion, the locations and sizes of the temperature reading areas are sensitively different for each approach as illustrated in the following table and the figure.

Technique	Resolution	Temperature reading location
Electrical method	Transistor Mean value	Active area of the device
IR microscopy	> 2 µm	Surface of the device (between Gate & Drain)
Raman spectroscopy	> 0.5 µm	Volume in GaN or GaAs layer
Thermoreflectance	> 1 µm	Surface of the device above the gate
3D Thermal simulation	< 0.1 µm	Maximum peak junction temperature (T_j)

Table 2: Comparison of temperature estimation techniques main features

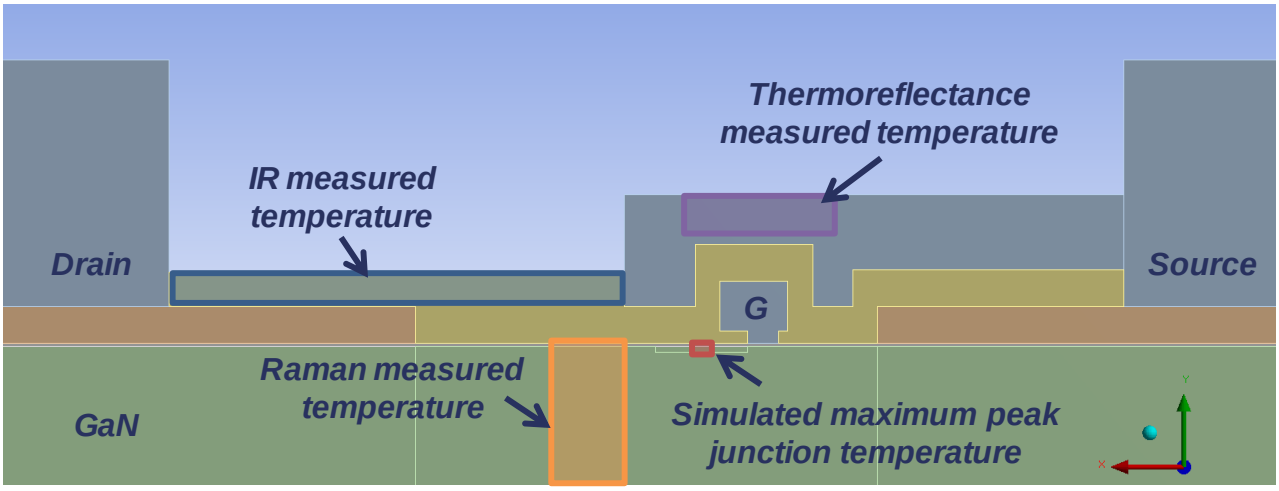

Fig. 3: Side view of the locations and sizes of the temperature reading areas in a GaN device. An averaged value is extracted during the measurement

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4. Impact of the method used for temperature evaluation on R_{th}

Because of the high heat flux in the active area of the device, a thermal gradient appears in the structure and the temperature quickly decreases around the gate finger area.

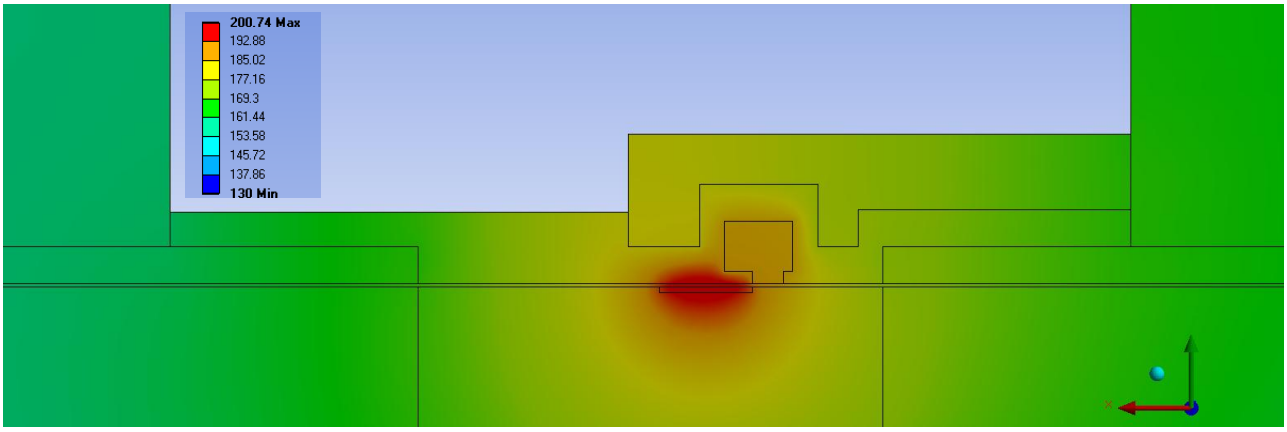

Fig. 4: Thermal gradient around the gate finger area of a GaN HEMT: Tb = 130 °C, Pdiss = 4 W

Therefore, the value of the thermal resistance can be very different depending on the method used to evaluate the temperature of the device under operating conditions. The thermal resistance obtained using one of the technique presented above is expressed as:

$$R_{th} = \frac{T_{read} - T_{ref}}{P_{diss}} \qquad \textit{Eq. 3}$$

Where T_{read} is the estimated temperature of the device using a specific method, T_{ref} is the reference temperature taken below the device ($T_{ref} = T_b$ in the case of a chip and $T_{ref} = T_c$ for the case of a packaged device), and P_{diss} is the total dissipated power in the device.

The table below gives a comparison of thermal resistance values obtained using different methods at identical T_{ref} and P_{diss}.

Technique	**GaN HEMT (8 x 125 µm)** **Tb = 130 °C / Pdiss = 4 W/mm**	**GaAS PHEMT (10 x 55 µm)** **Tb = 95 °C / Pdiss = 1 W/mm**
IR microscopy	10 °C/W	89 °C/W
Thermoreflectance	11 °C/W	96 °C/W
Raman spectroscopy	12.5 °C/W	118 °C/W
3D Thermal simulation	17.5 °C/W	149 °C/W

Table 3: Comparison of the thermal resistance estimation from different methods

The thermal resistance value depends strongly on the measurement method used to evaluate the temperature of the device under operating conditions. Depending on the method, the equivalent thermal resistance can be underestimated (up to 40 % in the examples given in table 3) when comparing to the one corresponding to the maximum peak junction temperature (T_j *from 3D thermal simulation*).

For the Life Time evaluation, the considered R_{th} is the one relative to the maximum peak junction temperature.

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5. Points of attention: Non-linearity of material thermal properties

The values of the thermal resistance mentioned in the UMS datasheets are calculated under specific operating conditions (Reference temperature and dissipated power).

Using this thermal resistance value for evaluating a junction temperature under other operating conditions (backside temperature and/or dissipated power) will lead to a slight missed estimation. This is due to the non-linear thermal properties of GaAs, GaN and SiC materials versus temperature. This phenomenon is illustrated in the figure below.

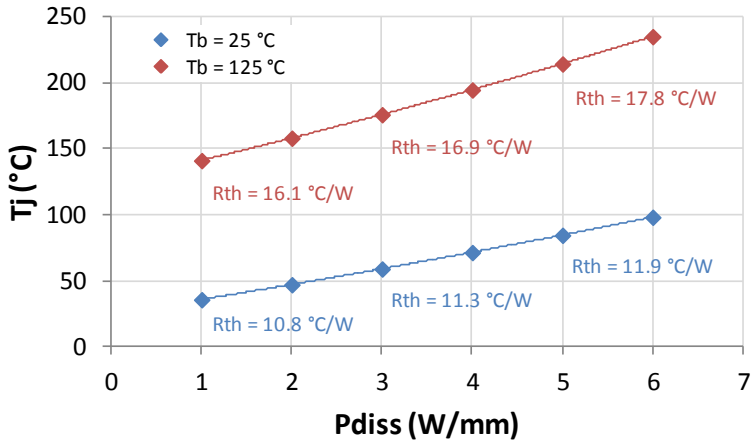

Figure 5: Impact of non-linear thermal properties of materials on T_j evaluation for a 8 x 125 µm GaN HEMT

It is therefore strongly recommended to evaluate accurately the thermal resistance (through measurement and/or 3D thermal simulation) of the complete assembly to obtain the right junction temperature under the right operating conditions.

6. Conclusion

The UMS methodology refers to the evaluation of the maximum peak junction temperature (T_j), based on 3D simulation results, calibrated with the different measurement methods described in this document. This methodology applies to all devices, die or packaged, GaAs or GaN based.

This is this methodology that is used for the qualification of the processes, based on specific qualification vehicles, leading to the activation energy and T_{50} evaluations.

For the products, die or packaged, an equivalent thermal resistance (R_{th_eq}) is provided, that allows customer to evaluate the reliability of the product within its environment.

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