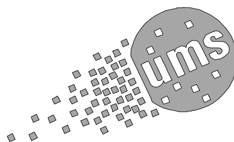

Application Note: THERMAL MANAGEMENT for DIES and PLASTIC PACKAGES

GaAs Monolithic Microwave IC

1. Introduction

Thermal management is key for proper usage of semi-conductors, and particularly III-V based circuits. Gallium Arsenide has very good microwave dielectric properties, with quite poor thermal conductivity as a counter part (at least compare to silicon). Thermal computation and simulation are then recommended to provide the requested thermal environment to a chip, from die-attach to package assembly, mother-board and housing design. Keeping the junction temperature below the defined T_{jmax} (maximum junction temperature) is mandatory to ensure reliability. This document aims to give an overview on thermal management at the chip level and also in plastic packages (QFN).
Basic rules, definitions and simplified methodologies are given here to help making temperature evaluation. There is no intention to replace precise and time consuming 3D physical thermal simulations. The real mechanical structure, the non linear thermal materials properties, the very large scale factors involved in an integrated circuit, especially from the transistors junctions (few nanometres) to the final chip housing (several millimetres), the coupling between the different hot areas will have also a strong effect on the final result.

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2. Thermal Management at the chip level

Two thermal sources exist at the chip level. The main source is coming from the transistor junctions and the second one is due to the resistive layers implemented on the circuit. The lifetime of the device is mainly driven by the junction temperature of the transistors and must be maintained as low as possible. The maximum junction temperature used by UMS for reliability and processes qualification is +175℃. Higher temperature should have an impact on the device reliability and lifetime. Guides lines to estimate this junction temperature are given below.

The thermal power dissipated by a transistor junction is (Pdissipated_J in Watts) defined by the simple expression Eq 1.

Eq 1 : Pdissipated_J(W) = Pdc(W) – [Pout_RF(W)-Pin_RF(W)]

Where:
Pdc (W) is the DC power consumption of the transistor junction= Vdc(Volts) x Idc (Amperes).
Vdc is the DC voltage applied to the junction.
Idc is the DC current flowing through the junction.
Pin_RF (W) is the input microwave power injected to the transistor junction in Watts.
Pout_RF (W) is the output microwave power emitted by the transistor junction in Watts.

Another expression can be defined around the Power Added Efficient (PAE in %) commonly used in electronic:

Eq 2 : PAE(%)=[Pout_RF(W)-Pin_RF(W)]/Pdc(W)

Then Eq 1 becomes:

Eq 3 : Pdissipated_J(W) =Pdc(W) x [1-PAE(%)]

The junction temperature must remain lower than a maximum limit defined according to the lifetime targeted for the device. Note that the safe estimation should be done considering the PAE=0% (No RF, CW mode) in most cases.

There is also thermal energy dissipated on chip due to the Joule effect through the resistive layers (metallic resistors …).
Then this dissipated power is defined with the very basic Joule equation:

Eq 4 : Pdissipated_R(W)=R(Ohms) x I^2 (Amperes).

Where:
R stands for the resistance of the concerned conductor in Ohms.

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I stand for the current flowing through the resistor in Amperes.

The total dissipated power $P_{dissipated}$ (W) at the chip level is the sum of all the thermal contributors:

Eq 5 : $$Pdissipated(W) = \sum_{junctions} Pdissipated_J(W) + \sum_{resistors} Pdissipated_R(W)$$

Due to the small dimensions of the devices, the distances between each of theses hot spots will induce thermal coupling and a rigorous analyse force to estimate each of these contributors and their coupled effects should be considered at the same time. But for a preliminary and simple estimation the following approximation can be done:

Each transistor constituted by several junctions can be considered as one single hot spot decoupled from the others transistors. It is assumed that all the junctions are strictly similar (same consumption, same PAE). Then the dissipated power of the transistor is given by:

Eq 6 : Pdissipated_T(W)=N x Pdissipated_J(W)
Pdissipated_T(W)=N x Pdc(W) x [1-PAE(%)]

Where N is the number of gates for the transistor.

The junction temperature of this stand alone component can be estimated by the following conductivity equation:

Eq 7 : Tj(℃)=[Pdissipated_T(W) x Rth $_{GaAs}$(℃/W)]+Tb(℃)

Where:
Tj (℃) is the junction temperature of a junction c onstituting the transistor considered.
Tb (℃) is the back side temperature of the chip.
Rth_{GaAs} (℃/W) is the thermal resistance equivalent to the semiconductor layer under the transistor.

This thermal resistance is function of several parameters and should be estimated with a rigorous 3D thermal simulation considering:

- The semiconductor physical properties
- The chip thickness
- The transistor geometry: via-holes location and shape, junctions spacing, metal drains, etc…

For a simple and quick first estimation, empirical rules can be used to determine this thermal resistance.

In the case of the UMS PHEMT processes (PH25 and PH15), Fig. 1 and Fig. 2 can be used to evaluate the thermal resistance of a FET (100µm GaAs substrate

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thickness), when the unit finger width Wu and package temperature (given as a parameter) are known.

R_{TH} is given for 1mm gate width. To obtain the thermal resistance R_{THC} of the component, the following formula can be used:

Eq 8: $Rth_{GaAs}(°C/W) = R_{TH}(°C.W^{-1}.mm) * 1000/W(\mu m)$

Where W is the total gate width of the FET.

Theoretical curves are based on FUKUI curves and are given for information purposes (H. FUKUI "Thermal Resistance Of GaAs Field-Effect Transistors", p118, IEDM, 1980).

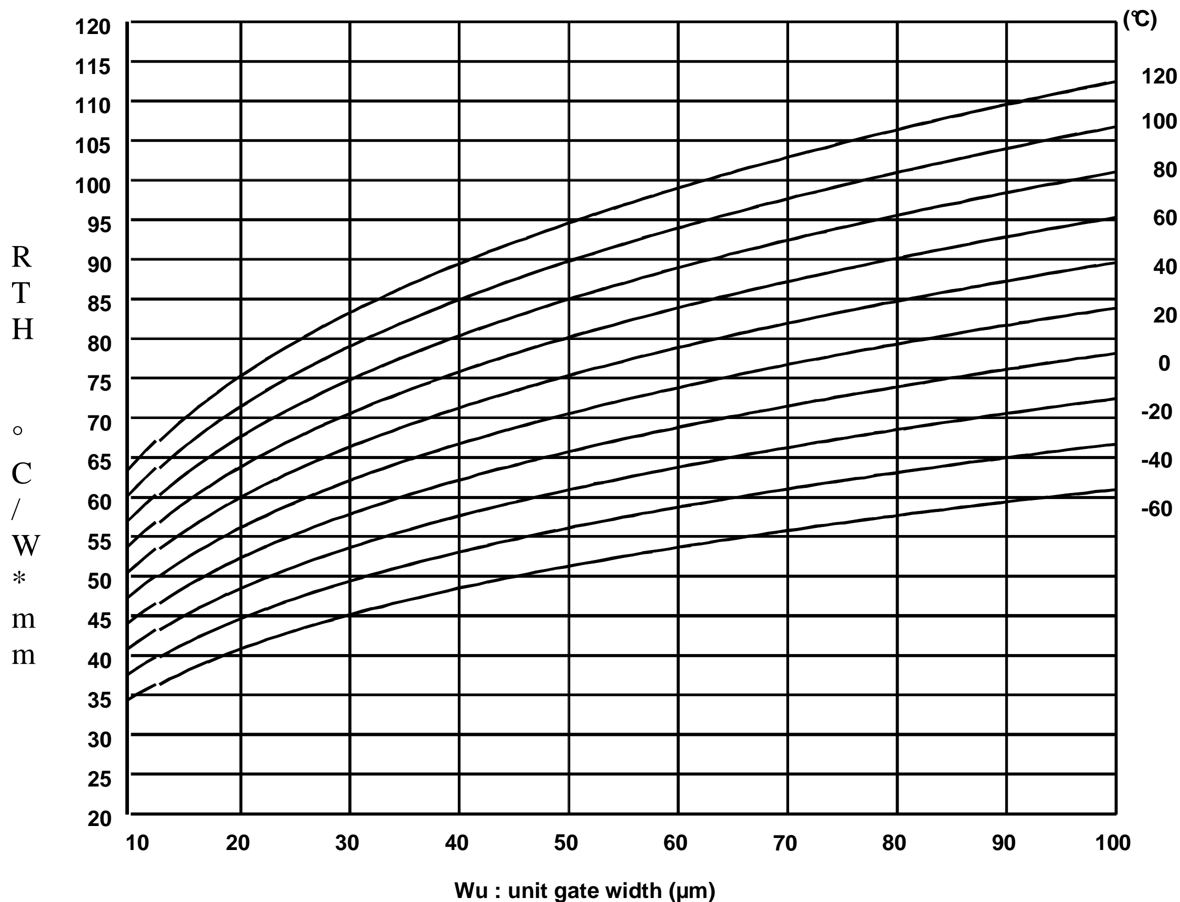

Fig. 1: Thermal resistance as a function of the unit gate width and chip back side temperature for the UMS PH25 process

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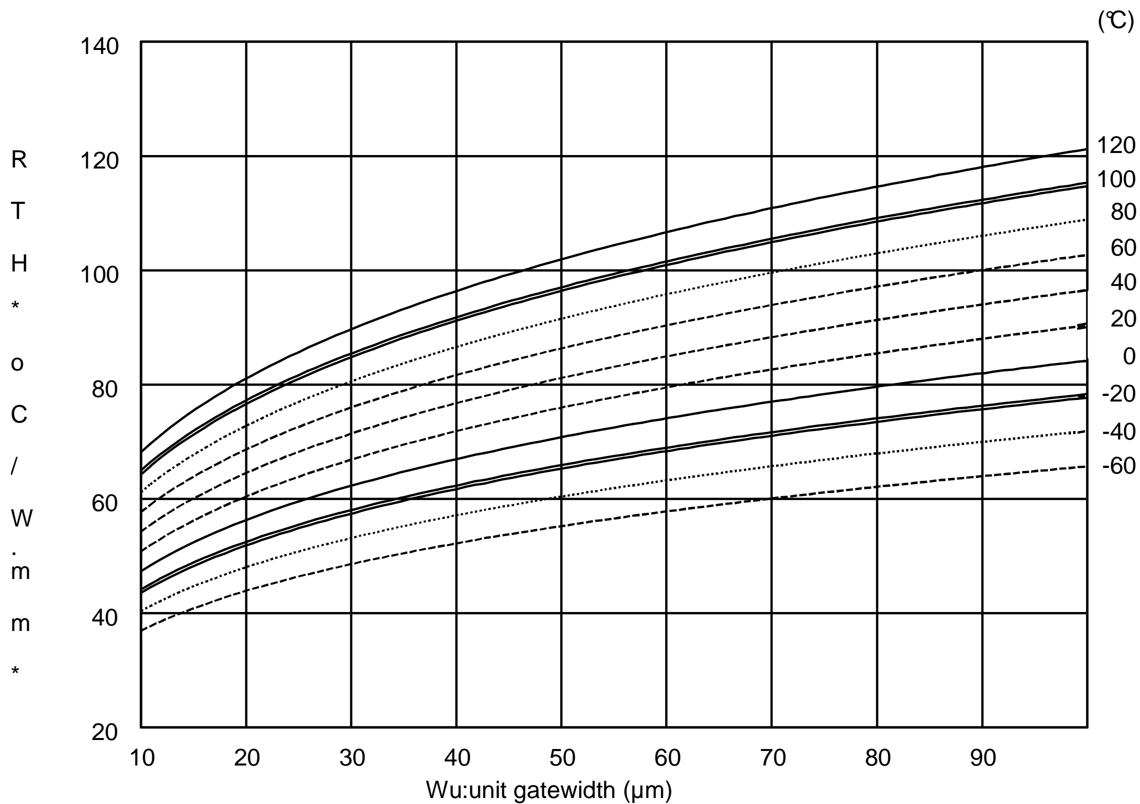

Fig. 2: Thermal resistance as a function of the unit gate width and chip back side temperature for the UMS PH15 process

3. Worst case estimation:

To estimate the real margins of the integrated circuit, the calculation of the junction temperature should be done for the worst operating conditions:

1. Maximum DC consumption.
2. For the circuit working with pulsed power supplies, the temperature estimation should be done in CW mode.
3. The reference temperature (chip back-side temperature or package back-side temperature) must be set-up to the maximum temperature specified for the equipment.
4. The microwave signal must be turned off (no RF signal injected to the function). Then the PAE = 0%.

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4. Thermal management for packaged product:

Physically, the GaAs chip is not assembled on a perfect heat spreader. Then, it is necessary to considered the whole structure from the die attach to the main thermal drain.
In this paragraph, the example of a die embedded in a plastic package assembled on a glass laminated carrier is considered. See Fig. 3 below.

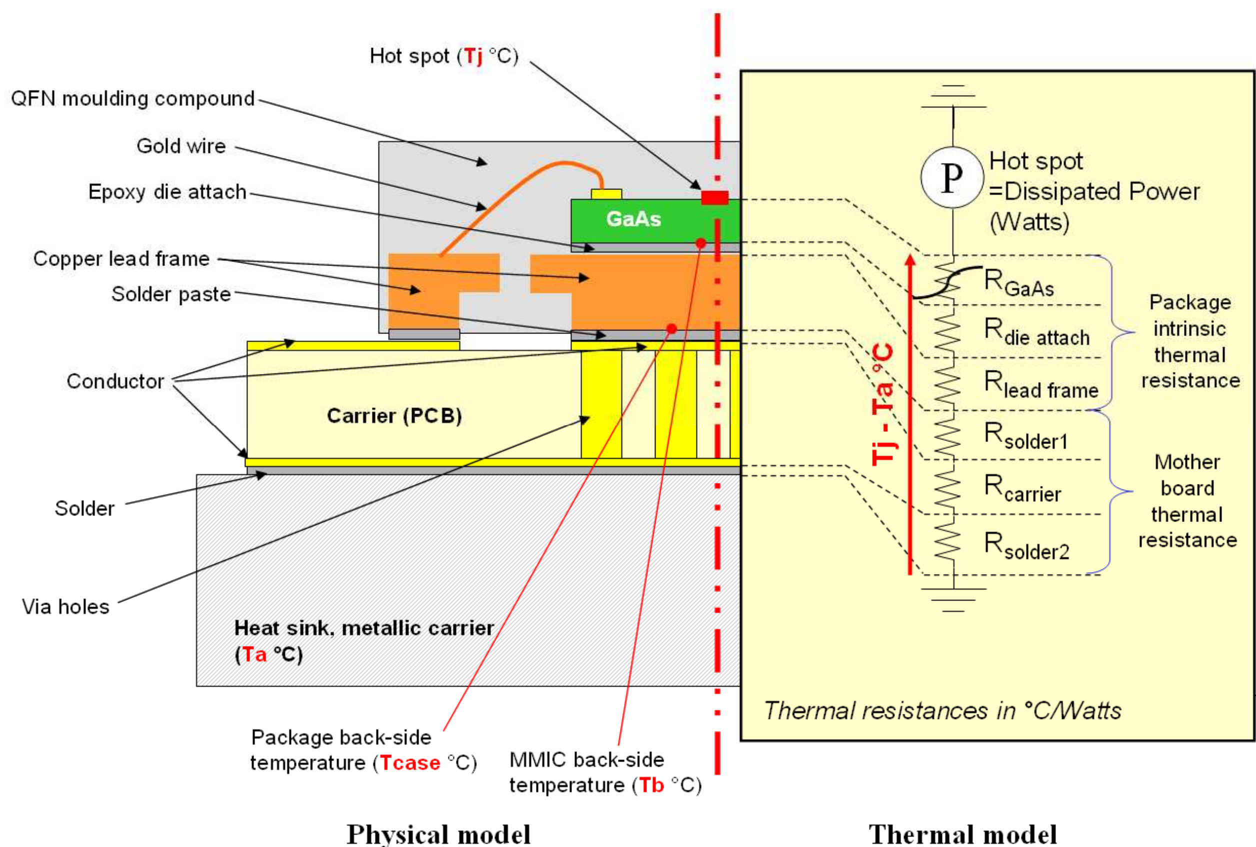

Fig. 3: Cross section of a QFN package assembled on the PCB & thermal model

At a first order, the main thermal limitations in this structure to dissipate the thermal power generated from the top side of the MMIC to the heat sink are coming from:

- The GaAs layer (R_{GaAs})
- The die attach layer ($R_{die\ attach}$)
- The carrier ($R_{carrier}$)

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The thermal resistance for each layer is given by Eq 9.

Eq 9 : $$R_{th}\left(\frac{°K}{W}\right)=\frac{1}{K_{th}\left(\frac{W}{m.°K}\right)}\times\frac{h(m)}{S(m^2)}$$

Where:
K_{th} is thermal conductivity of the layer.
h the thickness of the layer.
S is the section of the layer participating to the heat conduction.
The volume of the layer participating to the thermal conduction is estimated assuming that all the layer volume is used for the heat conduction (Volume(m^3) =h(m) x S(m²)). But in the reality, the thermal power will be conduced trough a dissipation cone where the opening angle (α) is a function of the materials thermal conductivities λ (see Eq 10 and
Fig. 4).

Eq 10 : $$\tan\alpha(Deg)=\frac{\lambda_1(W/m.°C)}{\lambda_2(W/m.°C)}$$

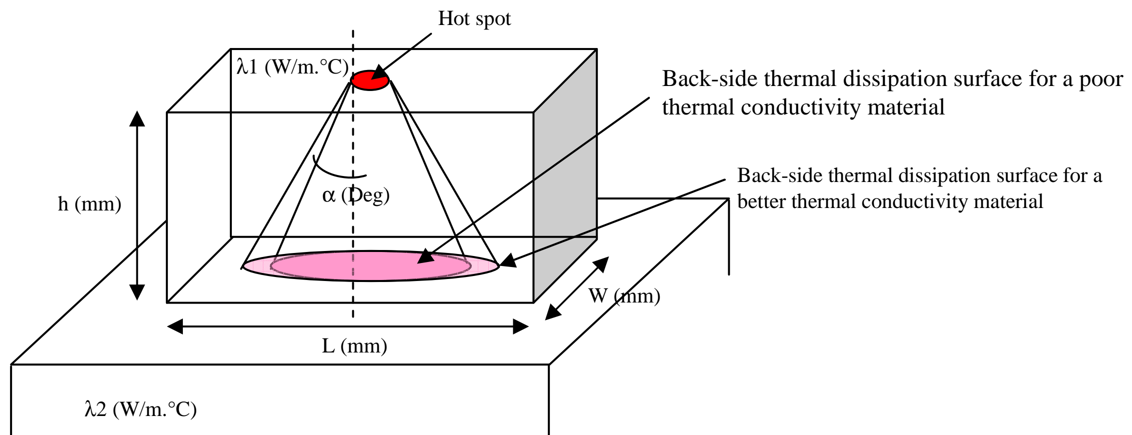

Fig. 4 : Thermal dissipation cone though an homogenous layer

Naturally, when the layer is thick enough the back-side dissipation surface is equivalent to the total layer surface S(mm²)=L x W as represented on Fig. 4.

However, to simplify the analyse in a first approximation it is possible to apply Eq 9 for the layers under the GaAs chip considering that all the contact surface between the layers will conduce the heat. That is due to the layers staking. Generally, the GaAs layer is the poorest thermal conductor in the structure because only a small

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volume of the crystal is used to spread out the thermal energy. This volume is limited by the dissipation cone defined at the Fig. 4. The die-attach and the lead-frame can be considered as good conductors. But the PCB mother board below this structure is generally limiting again. Then the angle α in Eq 10, will close to 90° in the die attach and in the lead-frame layers and reduced in the motherboard.

The temperature gradient ΔT(°C) through a layer flowing the dissipated power Pdissipated (W) is given bellow:

Eq 11 : $\Delta T(°C) = R_{th}\left(\frac{°C}{W}\right) \times Pdissipated(W)$

Then, the thermal model equivalent to the structure shown Fig. 3 is equivalent to Eq 12:

Eq 12:

$$\Delta T(°C) = T_j - T_a = (R_{GaAs} + R_{die_attach} + R_{lead_frame} + R_{solder1} + R_{carrier} + R_{solder2}) \times P_{dissipated}$$

$$\Delta T(°C) = T_j - T_a = Rth_{total} \times P_{dissipated}$$

$T_j - T_b = R_{GaAs} \times P_{dissipated}$ is the gradient of temperature through the MMIC.

$T_b - T_{case} = (R_{die_attach} + R_{lead_frame}) \times P_{dissipated}$ is the gradient of temperature through the package's base.

$T_{case} - T_a = (R_{solder1} + R_{carrier} + R_{solder2}) \times P_{dissipated}$ is the gradient of temperature through the PCB.

If we consider that the hot spot is constituted by a FET, $P_{dissipated}$ is given by the equation Eq 6. And T_j is the junction temperature as defined in Eq 7.

Thermal conductivities figures of some commonly used materials are collected in the following table.

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Materials	*Thermal conductivity Kth (W.m^{-1}.K^{-1})*	*CTE @ +25°C (ppm/K)*
GaAs crystal	44,3 @ T_0=+25°C [1]	5,73
Si	124	2,6
Quartz	1,4	0,59
Alumina (Al203 96%)	24 to 27,6	6,5 to 7
Alumina (Al203 99,8%)	36	8,4
Copper (Cu)	393,7	16,5
AlSiC	180	6.7
C194 (Copper alloy)	260	16
Aluminium	235	23,1
Gold	311 - 315	14,7
Ro4003	0,62	15
CuW/15-85	180	7
CuW/10-90	209	6.5
CuMo/15-85	184	6.6
Silva-K ™	110	7
BeO	250	6.4
Kovar	14	5.9
Molybdenum	140	5.1
FR4 or other PCB…	0,3	13-15
BCB	0,15 - 0,4	42
Speedboard Prepgreg	0,28	56
SN63 solder	50	-
Ablestick ABLETHERM 2600AT Epoxy die attach – high thermal performance epoxy (electrically conductive)	20	36 for T°<Tg 111 for T°>Tg (Tg=84°C)
Ablestick ABLEBOND 2815A Epxoy die attach – high thermal performance epoxy (electrically conductive)	20	64 fro T°<Tg 122 for T°>Tg (Tg=63°C)
Ablestick ABLEBOND 84-1 LMISR4 Epoxy die attach – low thermal performance epoxy (electrically conductive)	2,5	40 for T°<Tg 150 for T°>Tg (Tg=120°C)
Diemat DM6030Hk Epoxy die attach - high thermal performance epoxy (electrically conductive)	60	26
Ablestick ABLEBOND 84-3j Epoxy die attach (electrically non-conductive)	0,5	41 for T°<Tg 112 for T°>Tg (Tg=87°C)

Table 1: Materials physical properties

[1] The thermal conductivity of the GaAs crystal is non-linear and depends on temperature. For more precise calculations it is possible to use the following equations:

- Kth (W.m^{-1}.K^{-1}) = $55.9 \times 10^{3} * (273.15+To)^{-1.253}$
- Calorific Capacity (J/kg.K) = 330
- Density (kg/m3) = 5307

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4.1. The GaAs layer

For the transistors the contribution of the GaAs layer on the thermal dissipation can be estimated by applying the rules defined in the paragraph 2. Then R_{GaAs} in the equation Eq 12 can be substituted by the equation
Eq 8.

For a simple planar component such as a resistor, the GaAs crystal thermal conductivity given in the Table 1 must be considered to estimate R_{GaAs} with the equation Eq 9.

4.2. The die attach layer

The die attach layer should be as thin as possible to minimize the thermal resistance from the MMIC back-side to the package lead-frame. But the thickness must be calibrated to manage also the differential dilatations between the GaAs chip (CTE = 5.73 ppm/℃) and the copper lead-frame (CTE = 16.5 ppm/℃). Then, it is recommended to verify that the process used for this die attach will provide a void free layer: voids should be considered as insulators, and so not contributing to the heat conduction.
Typically the die attach thickness is between 10µm to 20µm depending on the MMIC surface.

4.3. The lead frame layer

The lead frame of the QFN packages is made of copper. This material has a very good thermal conductivity. So, the thermal power dissipated by the MMIC can be considered as fully spread through the entire die attach pad (DAP) surface. It can be considered as the closest heat sink from the MMIC. It is 200µm thick for typical QFN packages.

4.4. The solder layer

Typically, the thickness of the solder layer is about 20µm to 50µm and the thermal conductivity is close to 50 W/(m.°K).
Theses figures depend on the selected assembly process. And a special care must be taken in the soldering process to minimize the surface void in the solder.

4.5. The PCB (carrier layer)

The PCB constitutes a key point in the thermal design of the final product.
Typically UMS recommends using a glass-laminated carrier (Rogers 4003, thickness h = 203µm) to achieve high electrical performance and low cost product. To improve the thermal management through this layer, thermal via holes must be implemented. The density of the via-holes matrix and the fill-in material has to be considered to get the best thermal conductibility to the PCB.
The soldering process associated to carful PCB design is a key factor to minimize the voids under the package.

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The thermal resistance through the PCB can be approximated considering that all the thermal conduction is done by the via-holes metallization. The conduction through the substrate is then neglected.

This approximation is realistic if:

- The via-hole pitch (P_{via}) is not too large in comparison with the via-hole diameter (d_{via}).
    - Typically $P_{via}/d_{via} < 2.5$
- The via-hole is filled in with a low thermal resistive material (copper, solder paste, conductive glue). The equivalent via-hole thermal conductivity K_{via} has to be very high in comparison with the substrate thermal conductivity K_{sub}.
    - Typically $K_{via} > 100 \times K_{sub}$.

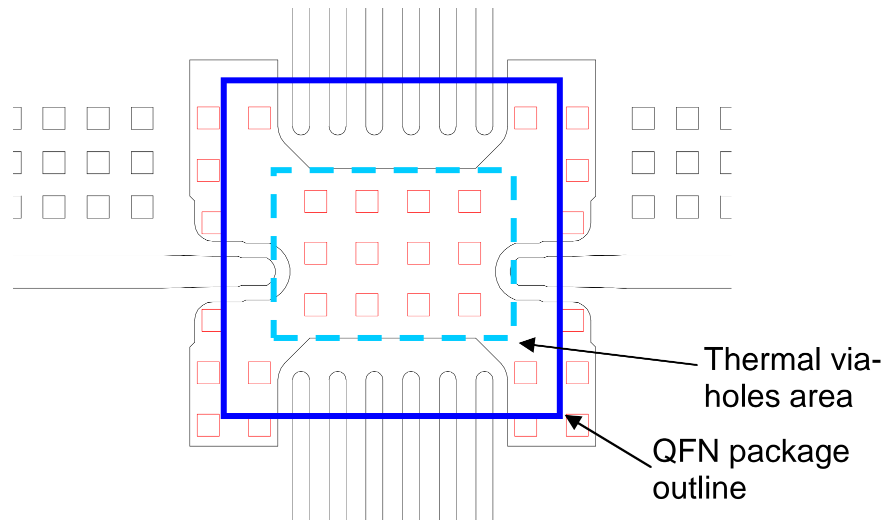

Fig. 5: Example of foot-print on PCB for QFN package

Then the PCB thermal resistance is given by:

Eq 13: $$Rth_{mother_board}\left(\frac{°K}{W}\right) = \frac{1}{K_{via}\left(\frac{W}{m.°K}\right)} \times \frac{h_{sub}(m)}{N_{via} \times \pi\left[\left(\frac{dext_{via}(m)}{2}\right)^2 - \left(\frac{d\,\mathrm{int}_{via}(m)}{2}\right)^2\right]}$$

Where:
K_{via} is the thermal conductivity of the fill-in material of the via-hole in W/(m.°K).
h_{sub} the substrate thickness in meters
N_{via} the number of via-holes under the die attach pad of the QFN package.
$dext_{via}$ the external via-holes diameter in meters.
$dint_{via}$ the internal via-holes diameter in meters.

Eq 13 based on Application Note «Thermal Management for Surface Mount Components» from Hittite Microwave.

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5. Thermal resistance for UMS standard QFN PLASTIC packages

	QFN 3X3	QFN4X4	QFN5X5
Package ground pad surface	1.45x1.45mm²	2.45x2.45mm²	3.65x3.65mm²
Thermal resistance equivalent to the die attach join: Surface and thermal resistance (Kth = 20 $W.m^{-1}.K^{-1}$)	2.89 mm² **0.24°C/W**	7.29 mm² **0.08°C/W**	13.32 mm² **0.04°C/W**
Thermal resistance equivalent to the die attach join: Surface and thermal resistance (Kth = 2.5 $W.m^{-1}.K^{-1}$)	2.89 mm² **1.9°C/W**	7.29 mm² **0.67°C/W**	13.32 mm² **0.3°C/W**
Package thermal resistance	**0.37°C/W**	**0.13°C/W**	**0.06°C/W**
Thermal resistance from the chip back-side to the package back-side (assuming die attach high conductibility 20 $W.m^{-1}. K^{-1}$)	**0.610°C/W**	**0.210°C/W**	**0.100°C/W**
Thermal resistance from the chip back-side to the package back-side (assuming die attach high conductibility 2.5 $W.m^{-1}. K^{-1}$)	**2.270°C/W**	**0.800°C/W**	**0.360°C/W**

Table 2: QFN plastic packages thermal resistance

6. Thermal limits

UMS has already demonstrated the capability of the plastic packages to handle high power levels. The maximum power handling reached up to now for ambient temperature lower than +75°C is:

Package type	***Dissipated power at ambient temperature = +75°C***
QFN 3 X 3 16 leads	1.7 W - CW
QFN 4 X 4 24 leads	3 W - CW
QFN 5 X 5 28 leads	>6 W – CW

Table 3: QFN plastic packages maximum dissipated power

The QFN final assembly will have a strong influence on the maximum dissipated power level acceptable by the device.

Remark:

The thermal figures given in this UMS' product data-sheet are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.

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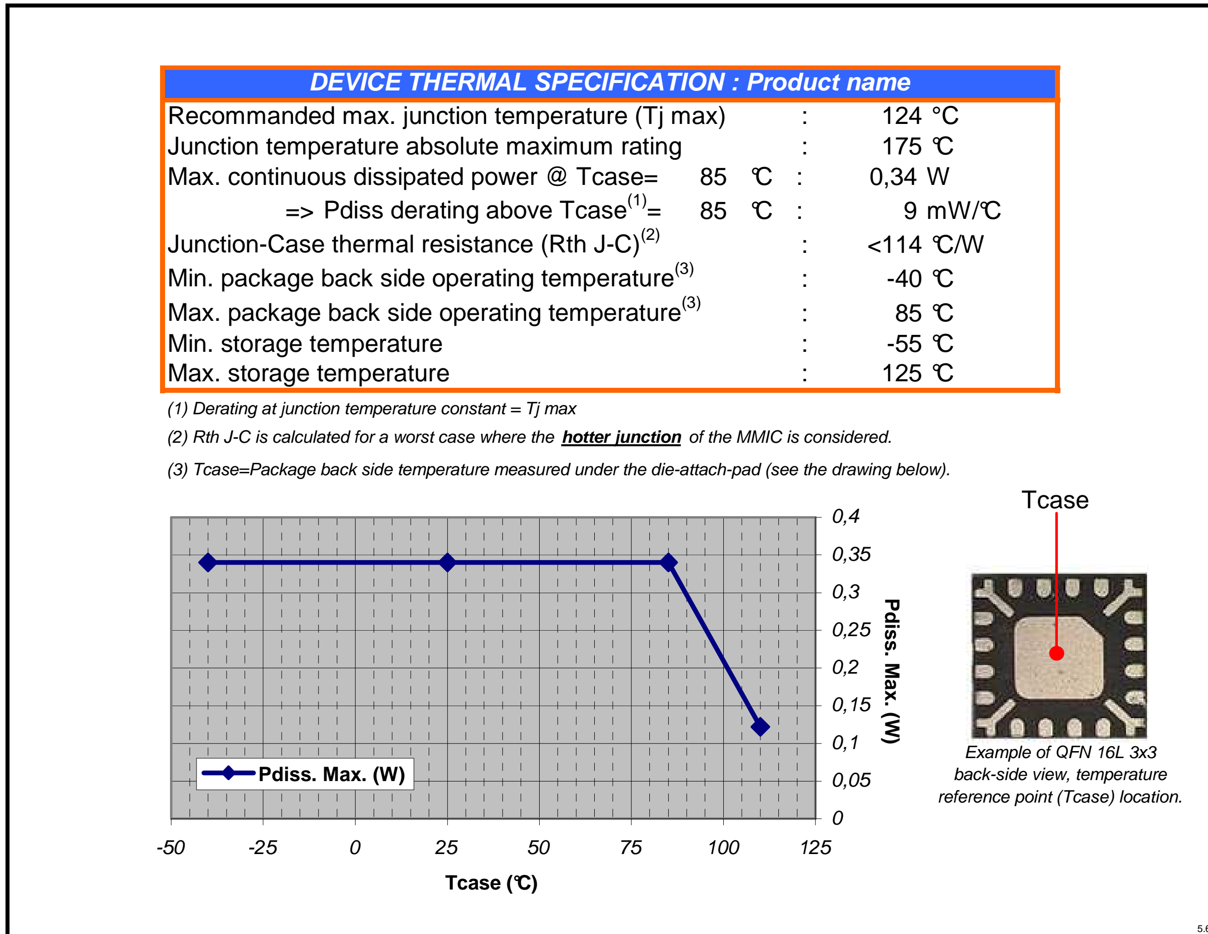
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table (Fig.6). So, the PCB should be designed to comply with this requirement.

A de-rating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss Max) in order to guarantee the nominal device life time (MTTF).



DEVICE THERMAL SPECIFICATION : Product name				
Recommanded max. junction temperature (Tj max)			:	124 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power @ Tcase=	85	°C	:	0,34 W
=> Pdiss derating above Tcase(1)=	85	°C	:	9 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<114 °C/W
Min. package back side operating temperature(3)			:	-40 °C
Max. package back side operating temperature(3)			:	85 °C
Min. storage temperature			:	-55 °C
Max. storage temperature			:	125 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).

Fig. 6: Thermal information sheet included to the UMS QFN product's data-sheet

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7. Example of junction temperature calculation

If we consider the Ku band driver described as below:

Output power at 1dB compression: Pout_P1dB = 30.5dBm
Linear gain: Gain = 28dB
Nominal positive supply voltage: Vd = +7V
Nominal positive supply current in linear mode: Id = 600mA
MMIC surface: 2300 x 1900µm^2

Biggest transistor: PHEMT 0.25µm 12 x 100µm
Maximum drain-source voltage: Vds = +7V
Maximum drain-source curent: Ids = +155mA
Transistor gain: G_FET = 9dB
FET output power at 1dB compression: P1dB_FET = 28dBm

Package: Plastic QFN 4x4 28 leads
Exposed ground paddle at the package bottom-side: 2700 x 2700µm^2
Equipment maximum operating temperature: Ta_max = +75℃

Mother board: Laminated substrate h = 0.203µm (Ro4003)
12 empty via-holes through the mother board.
The external via-holes diameter is = 300µm.
The internal via-holes diameter is = 260µm.
The via-hole platting is copper.

As a first approximation, the junction temperature of the largest transistor can be considered as the maximum temperature for the chip. The thermal coupling between the transistors is neglected.

The maximum dissipated power for the transistor is given by the equation Eq 6. In order to consider the worst thermal case, no microwave signal is applied to the function. Then all the DC prime power is dissipated by the transistor by thermal conduction and the PAE in Eq 6 equal 0%.

Then Eq 6 becomes: $P_{dissipated_}T(W)$ = Vds x Ids = 7V x 0.155A = 1.08W.

The considered structure is equivalent to the Fig. 3. The thermal resistance equivalent to the structure below the GaAs chip is calculated in the Table 4. Then the MMIC back-side temperature Tb can be estimated.

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Layers (see Fig. 3)		Length (µm)	Width (µm)	Thickness (µm)	Surface (mm²)	Material thermal conductivity ($W.m^{-1}.K^{-1}$)	Layer Rth (°C/W)	Used equation to calculate Rth	Thermal power flowing through the layers (W)	Top-side temperature (°C) see Eq 11
	Heat sink	-	-	-	-	-	0	Perfect conductor	1.08W	Ta=75
$R_{solder\ 2}$	Solder 2	2700	2700	20	7.29	50	0.05	Eq 9	1.08W	75.05
$R_{carrier}$	Mother board	-	-	-	-	-	2.44	Eq 13, considering 12 empty copper via-holes (external diameter=300µm, internal diameter=260µm), through a PCB of 203µm in thickness.	1.08W	77.69
$R_{solder\ 1}$	Solder 1	2700	2700	20	7.29	50	0.05	Eq 9	1.08W	77.74
$R_{lead\ frame}$	Copper lead-frame	2700	2700	200	7.29	393.7	0.07	Eq 9, considering that all the package exposed pad surface participates to the heat conduction	1.08W	77.81
$R_{die\ attach}$	Epoxy die attach	2300	1900	10	4.37	20	0.11	Eq 9, considering that all the chip back-side surface participates to the heat conduction	1.08W	**Tb=77.93**

+

$Rth_{total\ carrier}$ = 2.72 °C/W

Table 4: Carrier equivalent thermal resistance calculation (see Fig. 3)

The thermal resistance equivalent to the GaAs layer used in the Table 5 is estimated by using the Fig. 1, considering that the chip back side temperature is Tb = +77.93°C.

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Layers (see Fig. 3)		*Length (µm)*	*Width (µm)*	*Thickness (µm)*	*Surface (mm²)*	*Material thermal conductivity ($W.m^{-1}.°K^{-1}$)*	*Layer Rth (°C/W)*	*Used equation to calculate Rth*	*Following thermal power (W)*	*Top side Temperature (°C) see Eq 11*
Carrier *See* Table 4		-	-	-	-	-	2.72	Perfect conductor	1.08W	Tb=77.93
R_{GaAs}	GaAs FET	FET 12x 100µm PHEMT 0.25µm	=12x100	100	-	-	84.2	Eq 8 and Fig. 1 with Wu=100µm, Tb=+77.93°C, W=12x100µm	1.08W	**Tj=168.8**

\+

Rth_{total} = **86.92** **°C/W**

Table 5: Complete structure thermal resistance calculation (see Fig. 3)

Using the equation Eq 12, and assuming that the heat sink temperature is Ta = +75°C,

Tj(°C) = Rth $_{total}$ (°C/W) x Pdissipated_T(W)+Ta (°C)

Tj(°C) = 86.92 x 1.08 + 75 = 168.8°C.

The maximum acceptable junction temperature is given to be +175°C. (De-rating might apply for specific applications, such as Space).

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