

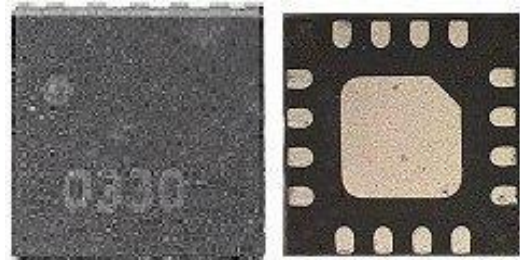
## 5-30GHz ATTENUATOR

GaAs Monolithic Microwave IC in SMD leadless package

### Description

The CHT4690-QAG is a variable 5-30GHz attenuator designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a MESFET process, 0.7 $\mu$ m gate length, via holes through the substrate and air bridges.

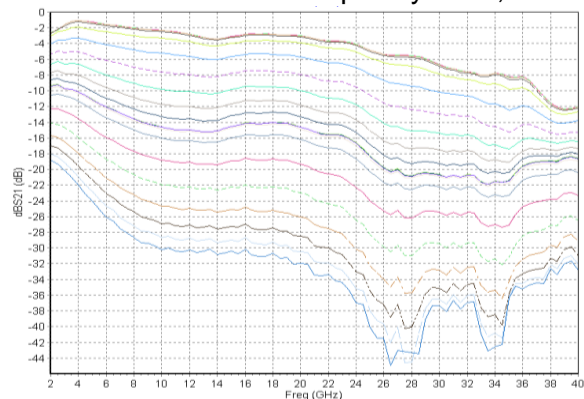


It is supplied in lead-free package.

### Main Features

- Broadband performance: 5-30GHz
- 25dBm typical input 1dB compression point (Any attenuation)
- 30dB dynamic range
- DC bias:  $-5V < V1 < 0V$  ;  $-5V < V2 < 0V$
- Package type: 16Leads QFN3x3

Attenuation versus frequency & V1, V2



### Main Characteristics

Temp. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	5		30	GHz
Min Att.	S21  (V1=-5V;V2=-5V) (10 to 24GHz)		4		dB
Max Att.	S21  (V1=0V;V2=0V) (10 to 30GHz)		35		dB
Pin1dB	Input 1dB compression point (any attenuation)		25		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

## Electrical Characteristics

Temp. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	5		30	GHz
Min Att.	S21  (V1=-5V;V2=-5V) (5 to 10GHz)		2	3	dB
	S21  (V1=-5V;V2=-5V) (11 to 24GHz)		4	5.5	dB
	S21  (V1=-5V;V2=-5V) (25 to 30GHz)		6	7.5	dB
Max Att.	S21  (V1=0V;V2=0V) (5 to 10GHz)	22	24		dB
	S21  (V1=0V;V2=0V) (11 to 30GHz)	28	35		dB
VSWRin	Input VSWR (any Att) (5 to 26GHz)		2.0:1		
VSWRout	Output VSWR (any Att) (6 to 26GHz)		2.5:1		
Pin1dB	Input 1dB compression point (any Att) (5 to 25GHz)	24	25		dBm
C/I3	C/I3 @ Pin/tone=12dBm (any Att) (to 26GHz)	36	40		dB
V1,V2	Voltage control range	-5		0	V

These values are representative of onboard measurements as defined on the drawing 96272 (see below).

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

## Absolute Maximum Ratings <sup>(1)</sup>

Temp. = 25°C

Symbol	Parameter	Values	Unit
V1	V1 control voltage	-6V to +0.6V	V
V2	V2 control voltage	-6V to +0.6V	V
Pin	RF input power	30	dBm
Ta	Operating temperature range (reference on ground paddle)	-40 to +95	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

## Typical Bias Conditions

at roomTemperature +25°C

Symbol	Pin No.	Parameter	Values	Unit
V1	6	V1 control voltage	-5 to 0	V
V2	7	V2 control voltage	-5 to 0	V

All other pins are not used for this device (but RFin: pin 3 and RFout: pin 10).

## Typical Sij results

Temp. = +25°C, V1 = -5V &amp; V2= -5V – Minimum attenuation

Freq GHz	dBS11 dB	PhS11 °	dBS12 dB	PhS12 °	dBS21 dB	PhS21 °	dBS22 dB	PhS22 °
2	-5,77	-130,20	-2,55	-31,72	-2,56	-31,77	-6,02	-122,20
3	-18,24	162,60	-1,56	-76,14	-1,57	-76,09	-16,23	-159,80
4	-33,75	-0,66	-1,05	-121,10	-1,05	-121,00	-28,33	-61,76
5	-18,99	-62,49	-1,27	-162,60	-1,28	-162,70	-17,03	-83,44
6	-15,80	-101,90	-1,53	159,00	-1,55	158,90	-14,97	-123,50
7	-14,81	-134,70	-1,74	120,90	-1,75	121,00	-14,59	-163,60
8	-14,79	-163,60	-1,99	83,83	-1,99	83,88	-15,92	150,90
9	-15,94	172,70	-2,20	47,44	-2,21	47,39	-18,83	93,77
10	-17,99	164,40	-2,29	10,91	-2,31	10,87	-20,83	8,96
11	-17,54	178,10	-2,49	-26,01	-2,51	-26,06	-16,58	-75,82
12	-13,70	167,20	-2,76	-62,82	-2,77	-62,74	-12,70	-127,80
13	-12,17	146,50	-3,17	-98,13	-3,19	-98,10	-10,52	-167,80
14	-11,15	119,70	-3,37	-130,70	-3,37	-130,60	-9,67	157,20
15	-12,30	86,70	-3,08	-164,50	-3,09	-164,40	-10,23	120,20
16	-15,11	52,00	-2,82	159,70	-2,81	159,70	-12,39	89,50
17	-21,56	13,96	-2,74	123,00	-2,77	122,80	-15,62	59,38
18	-30,69	-31,65	-2,82	86,43	-2,81	86,37	-22,70	53,56
19	-28,59	-144,80	-2,88	50,32	-2,88	50,19	-23,35	49,99
20	-32,47	147,50	-2,98	13,16	-2,99	13,04	-28,06	52,01
21	-34,58	-83,05	-3,35	-24,26	-3,36	-24,34	-22,49	52,93
22	-27,02	-107,30	-3,64	-59,80	-3,65	-59,89	-17,98	14,05
23	-25,65	-58,89	-3,67	-97,53	-3,68	-97,70	-15,16	-14,18
24	-14,56	-81,43	-4,08	-138,10	-4,07	-138,50	-11,33	-37,63
25	-11,52	-119,30	-4,83	-177,20	-4,84	-177,50	-8,30	-68,74
26	-11,89	-145,10	-5,32	145,60	-5,35	145,70	-7,08	-96,79
27	-13,87	-157,20	-5,49	107,70	-5,46	107,70	-7,17	-120,00
28	-15,40	-137,70	-5,52	67,12	-5,53	66,95	-8,14	-131,80
29	-11,70	-124,90	-5,87	24,50	-5,88	24,46	-8,03	-132,80
30	-7,47	-137,50	-6,63	-15,21	-6,63	-15,33	-6,28	-139,50
31	-5,43	-163,20	-7,15	-52,23	-7,16	-52,16	-4,96	-153,40
32	-4,86	173,10	-7,59	-88,55	-7,57	-88,62	-4,23	-172,40
33	-5,41	146,80	-7,96	-125,00	-7,97	-125,30	-5,17	167,20
34	-9,51	122,00	-7,74	-160,70	-7,75	-160,80	-6,42	164,50
35	-12,43	169,50	-8,22	159,30	-8,21	159,30	-6,74	152,80
36	-6,67	164,80	-8,15	120,10	-8,13	119,90	-7,16	159,50
37	-3,78	142,10	-9,68	77,59	-9,65	77,40	-4,40	153,60
38	-2,85	120,90	-11,55	46,82	-11,57	47,05	-2,89	134,90
39	-2,31	103,00	-12,30	21,67	-12,29	21,81	-2,40	116,80
40	-2,25	84,05	-12,06	-4,80	-12,05	-5,05	-2,35	99,67

Refer to the “definition of the Sij reference planes” section below

## Typical Sij results

Temp. = +25°C, V1 = 0V & V2= 0V – Maximum attenuation

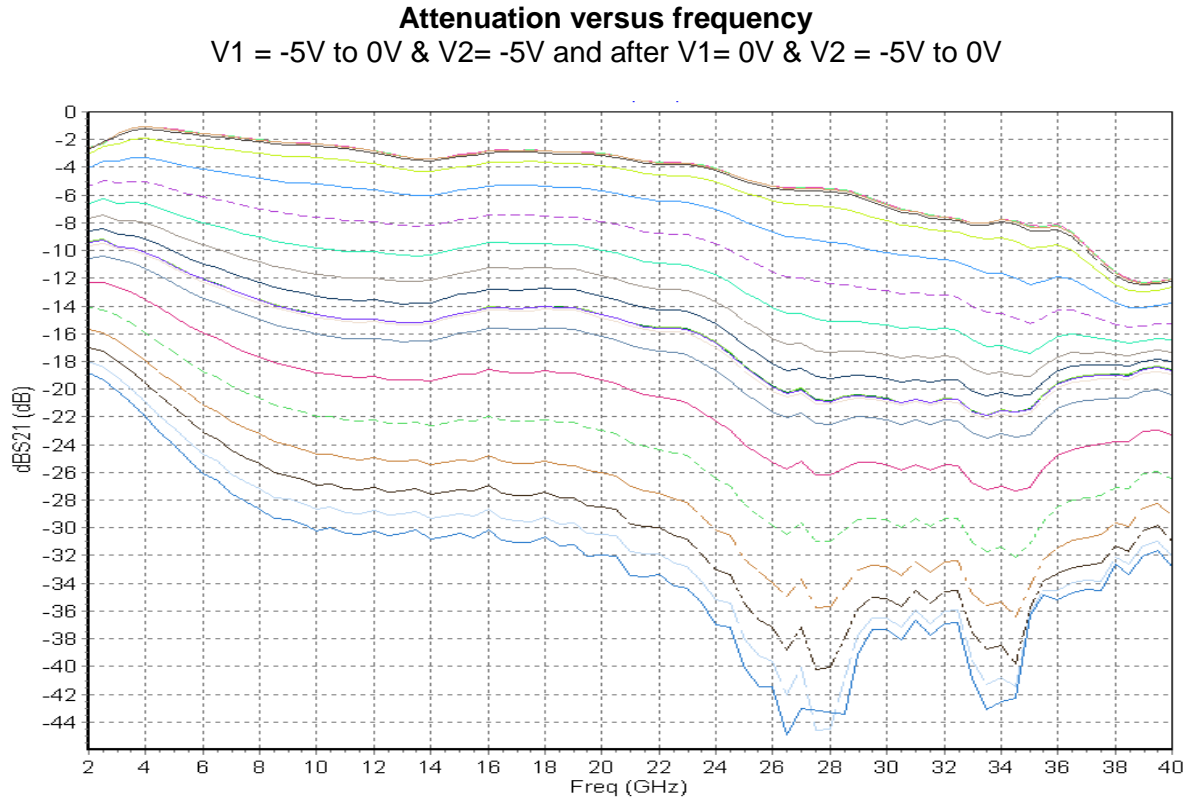
Freq GHz	dBS11 dB	PhS11 °	dBS12 dB	PhS12 °	dBS21 dB	PhS21 °	dBS22 dB	PhS22 °
2	-4,58	-164,60	-18,83	-43,68	-18,87	-43,73	-2,67	-145,10
3	-7,66	152,60	-20,15	-106,60	-20,15	-106,10	-4,26	173,60
4	-10,04	125,10	-22,05	-156,40	-22,01	-156,00	-5,39	143,20
5	-11,79	106,80	-24,07	159,40	-24,02	158,80	-6,30	118,80
6	-13,15	92,84	-25,94	120,10	-26,08	119,30	-7,03	98,09
7	-13,93	83,62	-27,50	81,83	-27,53	82,42	-7,74	79,64
8	-14,30	74,01	-28,73	45,60	-28,64	46,65	-8,37	62,86
9	-14,51	62,94	-29,57	11,40	-29,38	11,36	-8,98	47,10
10	-14,69	50,17	-30,02	-20,80	-30,21	-21,85	-9,58	32,09
11	-15,36	36,83	-30,34	-52,88	-30,36	-52,20	-10,35	17,49
12	-15,66	19,40	-30,51	-84,12	-30,19	-84,48	-10,98	2,35
13	-16,00	-1,97	-30,52	-115,70	-30,43	-117,50	-11,49	-13,07
14	-16,07	-25,88	-30,75	-147,80	-30,77	-147,00	-11,91	-28,88
15	-16,04	-50,59	-30,52	-176,60	-30,41	-174,50	-12,25	-44,35
16	-15,58	-74,18	-30,43	152,20	-30,14	152,40	-12,33	-59,58
17	-14,97	-95,76	-31,02	124,00	-31,02	120,70	-12,29	-73,43
18	-14,41	-114,50	-31,05	98,24	-30,67	100,30	-12,01	-86,90
19	-14,10	-129,00	-31,54	69,96	-31,22	69,87	-11,72	-99,34
20	-13,91	-141,20	-32,25	43,99	-31,96	42,11	-11,36	-110,20
21	-14,02	-150,70	-33,24	15,69	-33,43	17,32	-11,07	-120,00
22	-14,48	-156,50	-33,48	-1,81	-33,39	1,40	-10,67	-128,10
23	-14,56	-155,60	-34,63	-31,43	-34,36	-32,15	-10,37	-135,30
24	-14,08	-157,40	-36,28	-54,07	-36,96	-57,05	-9,91	-143,00
25	-13,59	-156,60	-39,81	-82,06	-40,15	-79,86	-9,65	-149,40
26	-12,69	-155,60	-42,40	-102,50	-41,47	-100,20	-9,37	-155,30
27	-11,18	-159,80	-43,51	-159,90	-43,00	-166,90	-8,98	-161,40
28	-10,24	-166,20	-48,88	115,70	-48,73	104,20	-8,75	-168,00
29	-9,49	-174,10	-38,50	48,99	-39,12	48,98	-8,56	-175,10
30	-9,05	177,40	-37,50	-8,61	-37,33	-6,80	-8,31	178,00
31	-8,24	169,60	-36,97	-33,24	-36,66	-31,20	-8,16	170,50
32	-7,73	158,70	-37,26	-61,32	-36,88	-63,10	-8,13	162,70
33	-7,12	146,60	-40,29	-100,10	-40,91	-102,40	-8,02	154,70
34	-7,28	132,60	-43,01	-79,19	-42,57	-80,83	-7,87	147,80
35	-7,33	122,70	-36,51	-71,50	-36,30	-73,28	-7,15	135,70
36	-7,18	112,10	-34,73	-122,50	-35,16	-125,70	-7,61	122,30
37	-7,17	100,40	-34,58	-154,40	-34,46	-157,00	-8,13	115,00
38	-7,32	91,06	-33,21	174,60	-32,59	173,20	-8,04	108,70
39	-7,32	83,47	-32,28	135,30	-32,07	131,80	-7,60	99,93
40	-7,28	75,23	-32,57	101,40	-32,78	105,50	-7,70	90,76

Refer to the “definition of the Sij reference planes” section below

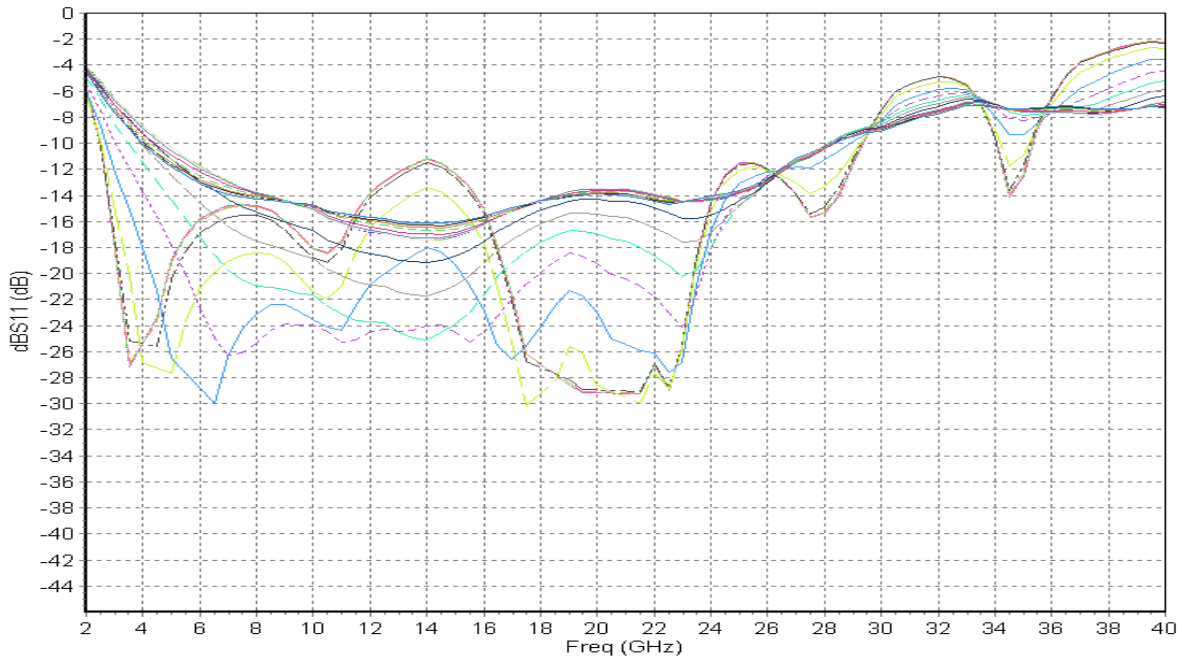
## Typical Results

Temp. = +25°C

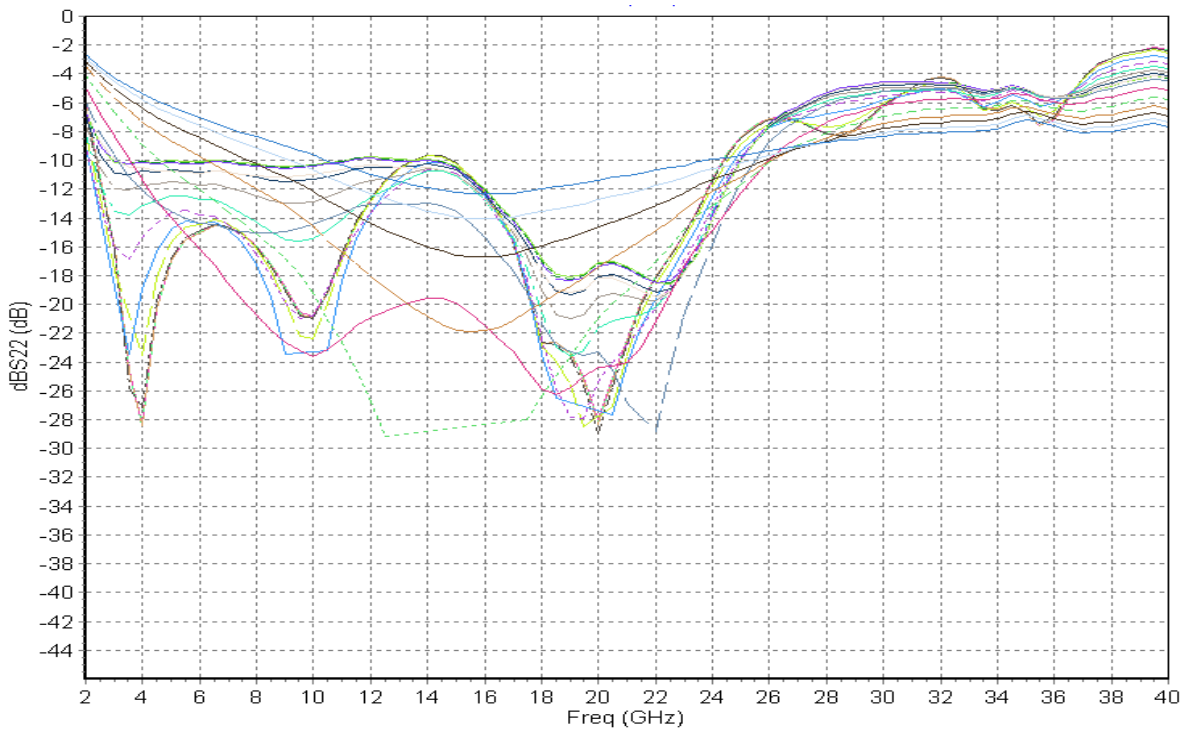
Measurements performed in the package access, using the proposed land pattern & board 96272.



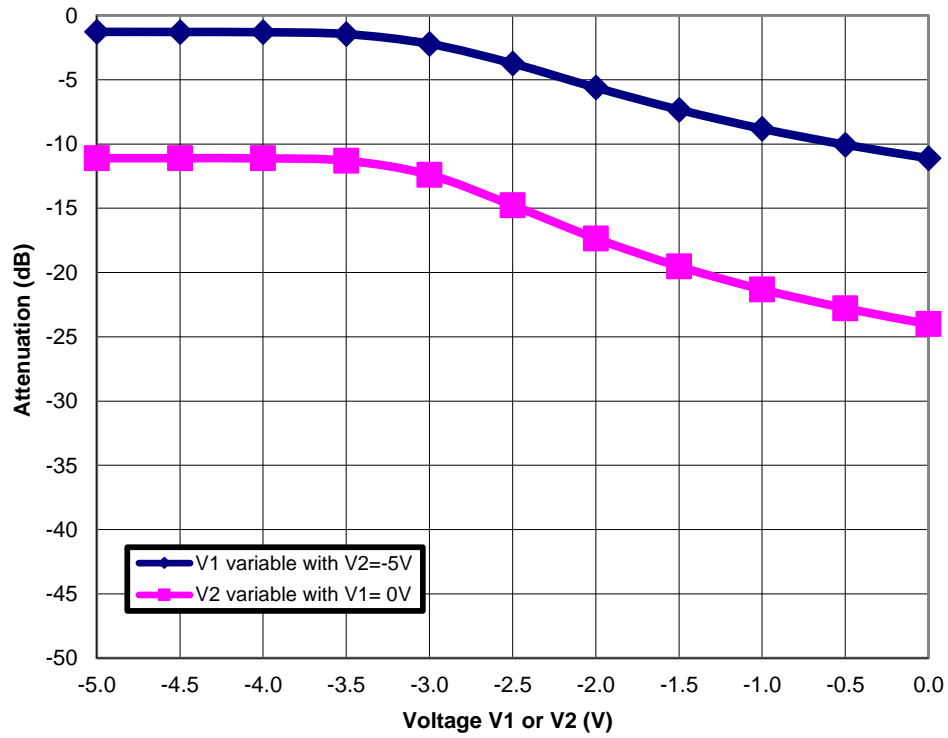
### Input Return loss versus frequency for total attenuation range



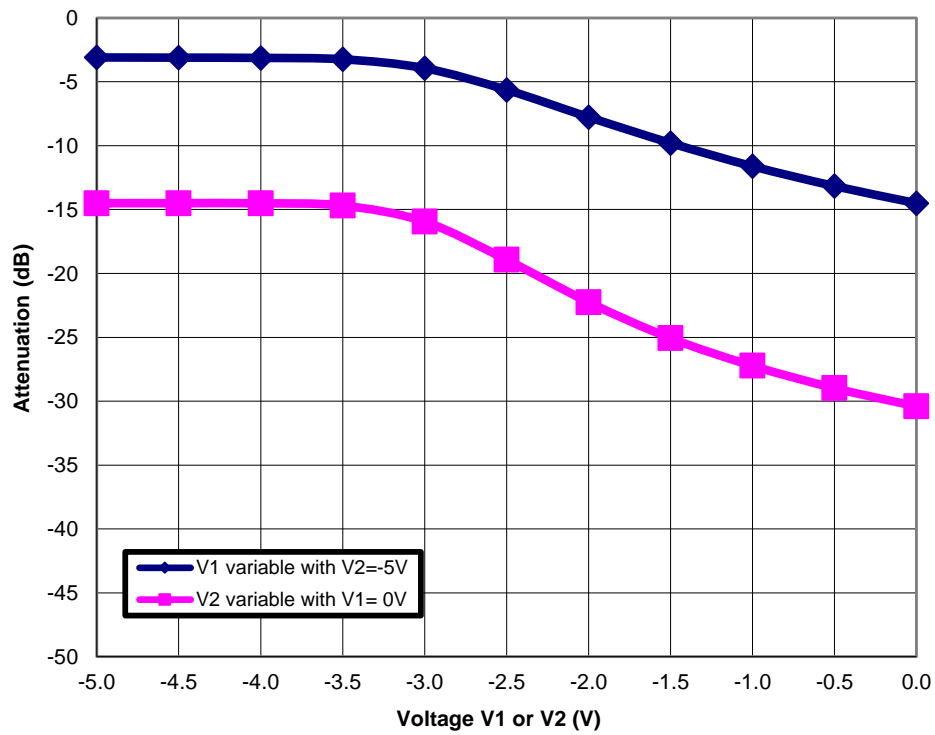
### Output Return loss versus frequency for total attenuation range



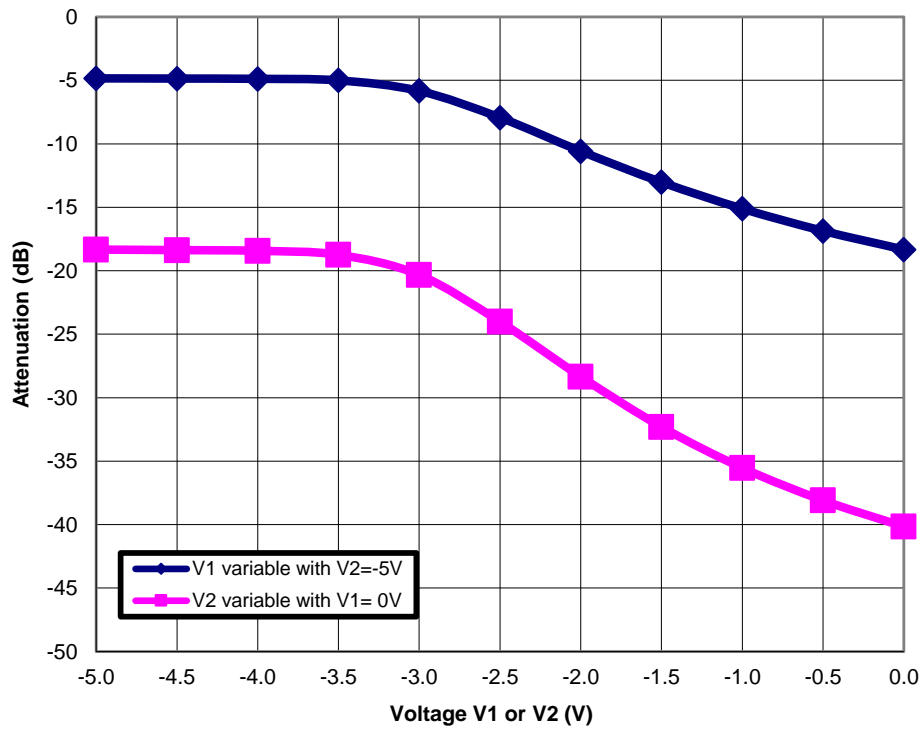
Attenuation control at 5GHz



Attenuation control at 15GHz

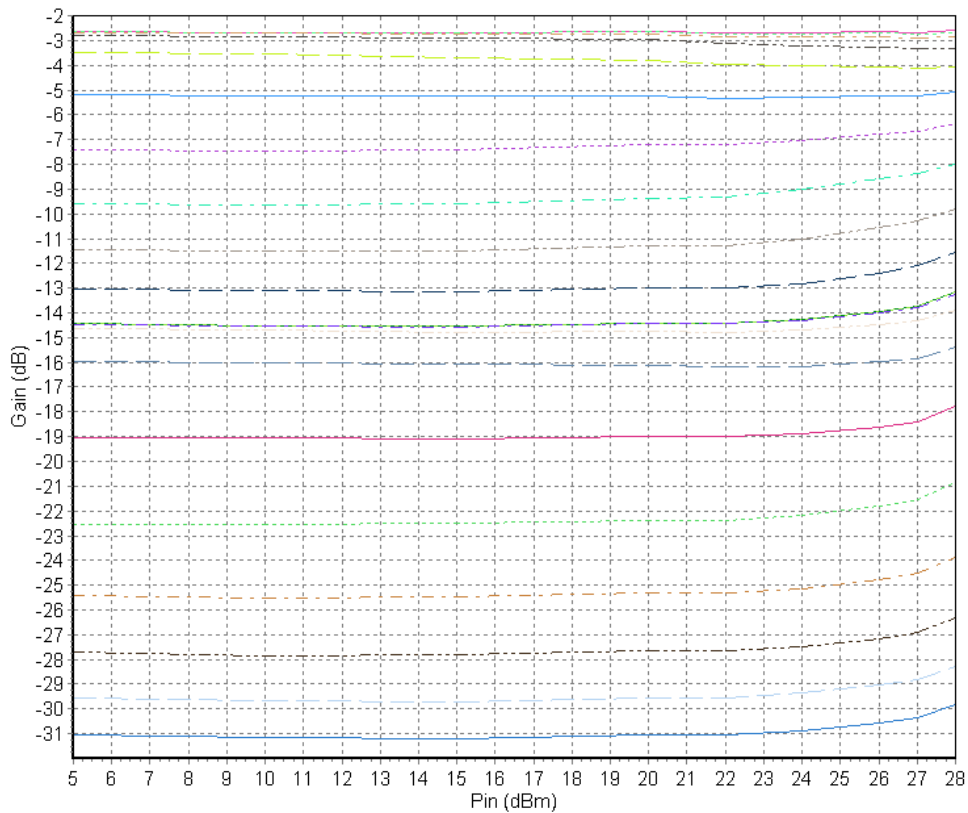


## Attenuation control at 25GHz



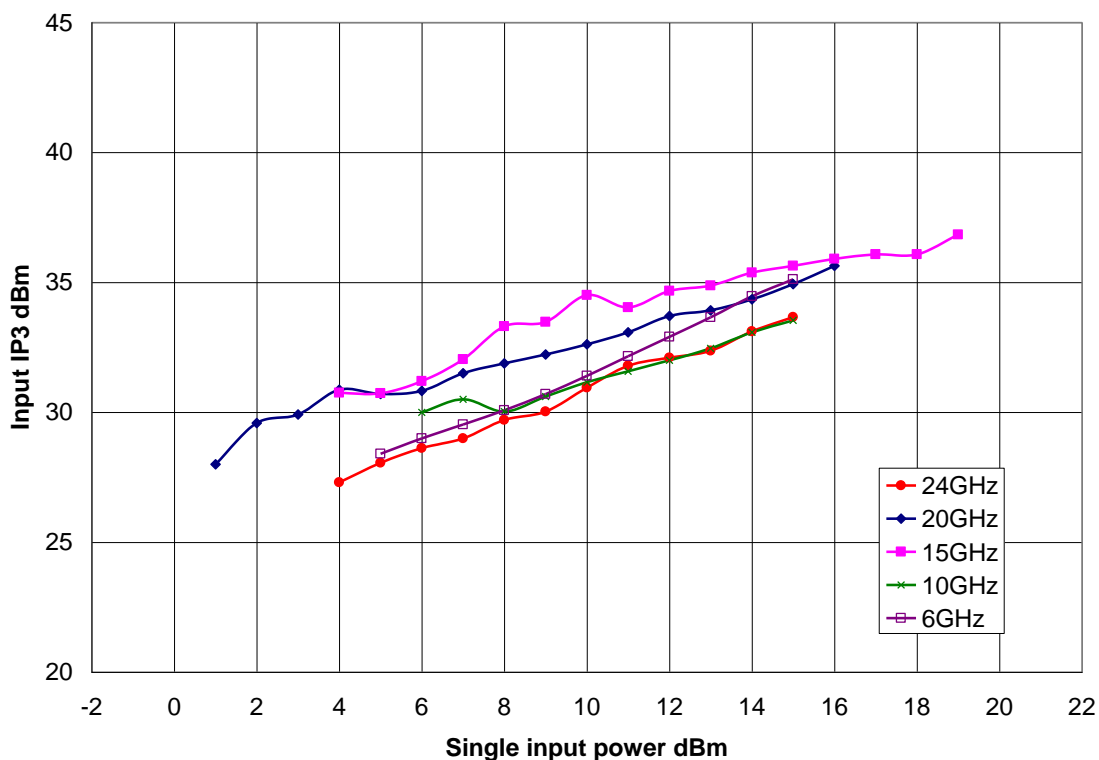
## Attenuation versus input power @ 15GHz

V1 = -5V to 0V & V2 = -5V and after V1 = 0V & V2 = -5V to 0V

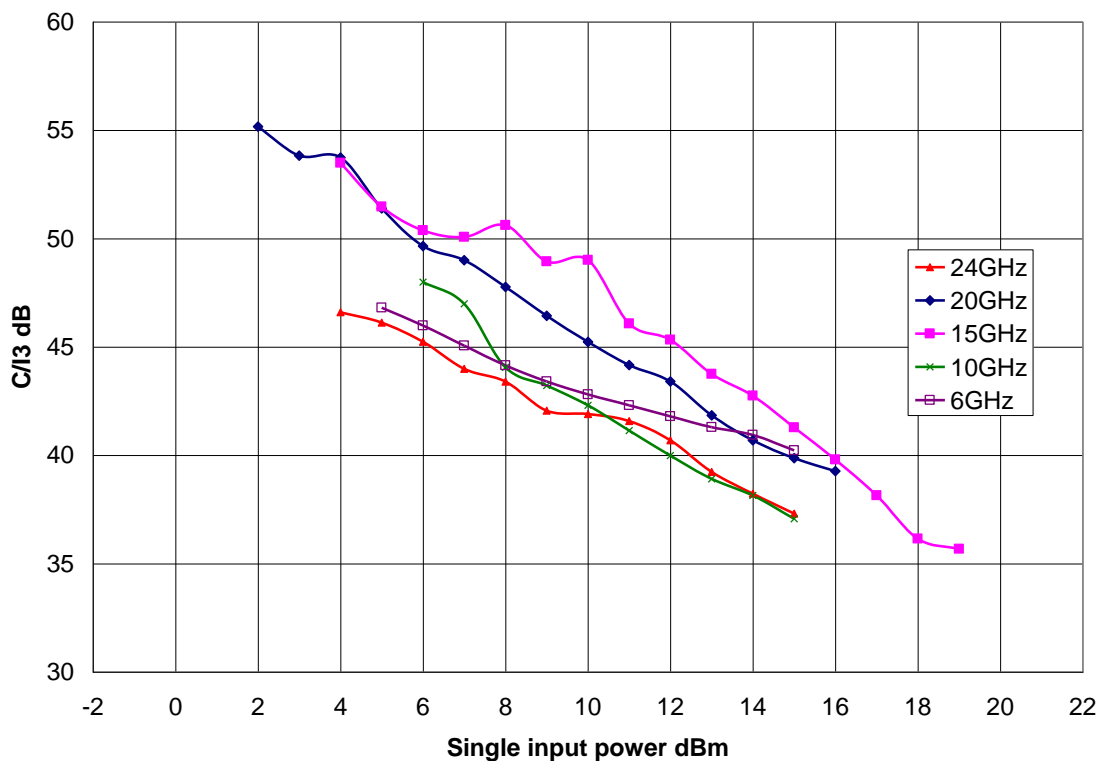




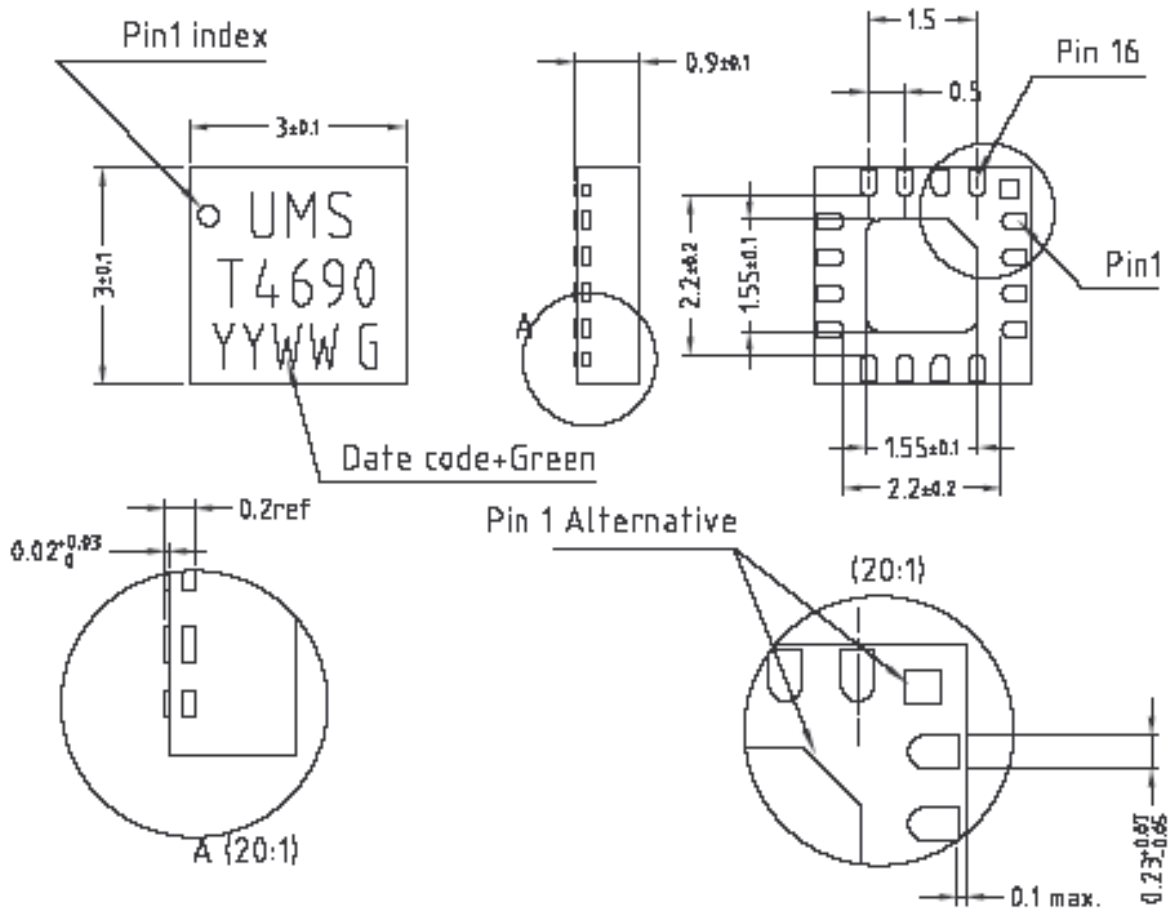
**Input IP3 versus input power**  
 V1 = -3.5V & V2= -5V (worst case area for the linearity)



**C/I3 versus input power**  
 V1 = -3.5V & V2= -5V (worst case area for the linearity)



Package outline:



Matt tin, Lead free (Green)

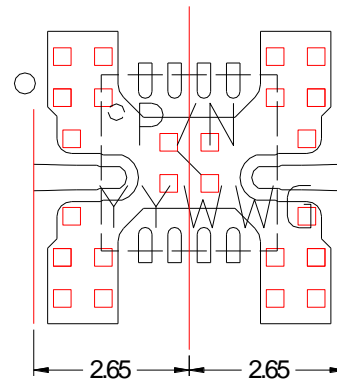
Units : mm

From the standard : JEDEC MO-220

- |          |            |
|----------|------------|
| 1- NC    | 9- Gnd     |
| 2- Gnd   | 10- RF Out |
| 3- RF In | 11- Gnd    |
| 4- Gnd   | 12- Nc     |
| 5- Nc    | 13- Nc     |
| 6- V1    | 14- Nc     |
| 7- V2    | 15- Nc     |
| 8- Nc    | 16- Nc     |

## Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board 95542 shown below. The reference is the symmetrical axis of the package. The input and output reference planes are located at 2.65mm offset (input wise and output wise respec.) from this axis. Then, the given Sij incorporates this land pattern.



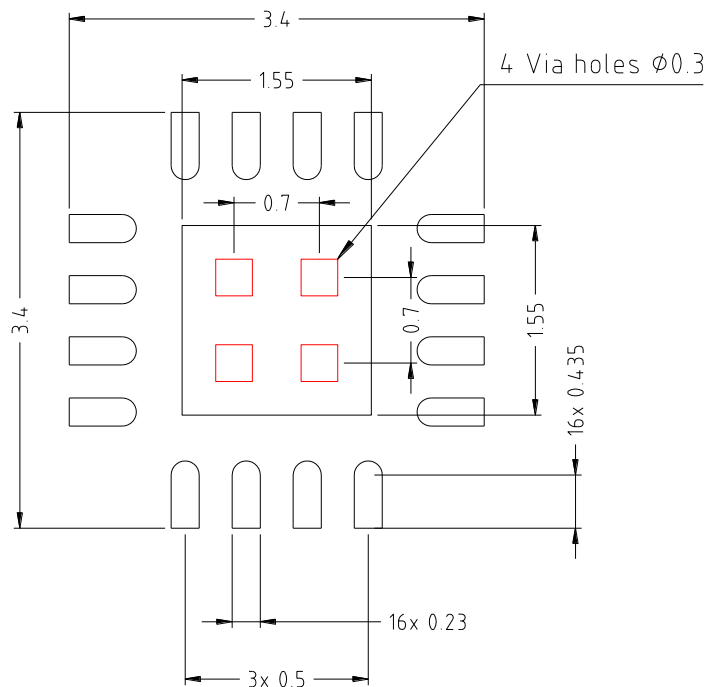
## Application note

The design of the motherboard has a strong impact on the over all performance since the transition from the motherboard to the package is comparably large. In case of the SMD type packages of United Monolithic Semiconductors the motherboard should be designed according to the information given in the following to achieve good performance. Other configurations are also possible but can lead to different results. If you need advise please contact United Monolithic Semiconductors for further information.

SMD type packages of UMS should allow design and fabrication of micro- and mm-wave modules at low cost. Therefore, a suitable motherboard environment has been chosen. All tests and verifications have been performed on Rogers RO4003. This material exhibits a permittivity of 3.38 and has been used with a thickness of 200µm [8 mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line has a strip width of about 460µm [approx. 18 mils].

The contact areas on the motherboard for the package connections should be designed according to the footprint given below. The proper via structure under the ground pad is very important in order to achieve a good RF and lifetime performance. All tests have been done by using a grid of plated through vias with a diameter of less than 300µm [12 mils] and a spacing of less than 700µm [28 mils] from the centres of two adjacent vias. The via grid should cover the whole space under the ground pad and the vias closest to the RF ports should be located near the edge of the pad to allow a good RF ground connection. Since the vias are important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between package and heat sink. For power devices the use of heat slugs in the motherboard instead of a grid of via's is recommended.

For the mounting process the SMD type package can be handled as a standard surface mount component. The use of either solder or conductive epoxy is possible. The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils]. Caution should be taken to obtain a good and reliable contact over the whole pad areas. Voids or other improper connections, in particular, between the ground pads of motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.



*(For production, design must be adapted with regard to PCB tolerances and assembly process)*

### Basic footprint for a 16L-QFN3x3 (all units mm)

(Please, refer to the UMS proposed footprint for optimum operation in the following "Proposed Assembly board" section)

The RF ports are DC blocked on chip. The DC connections (V1,V2) do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

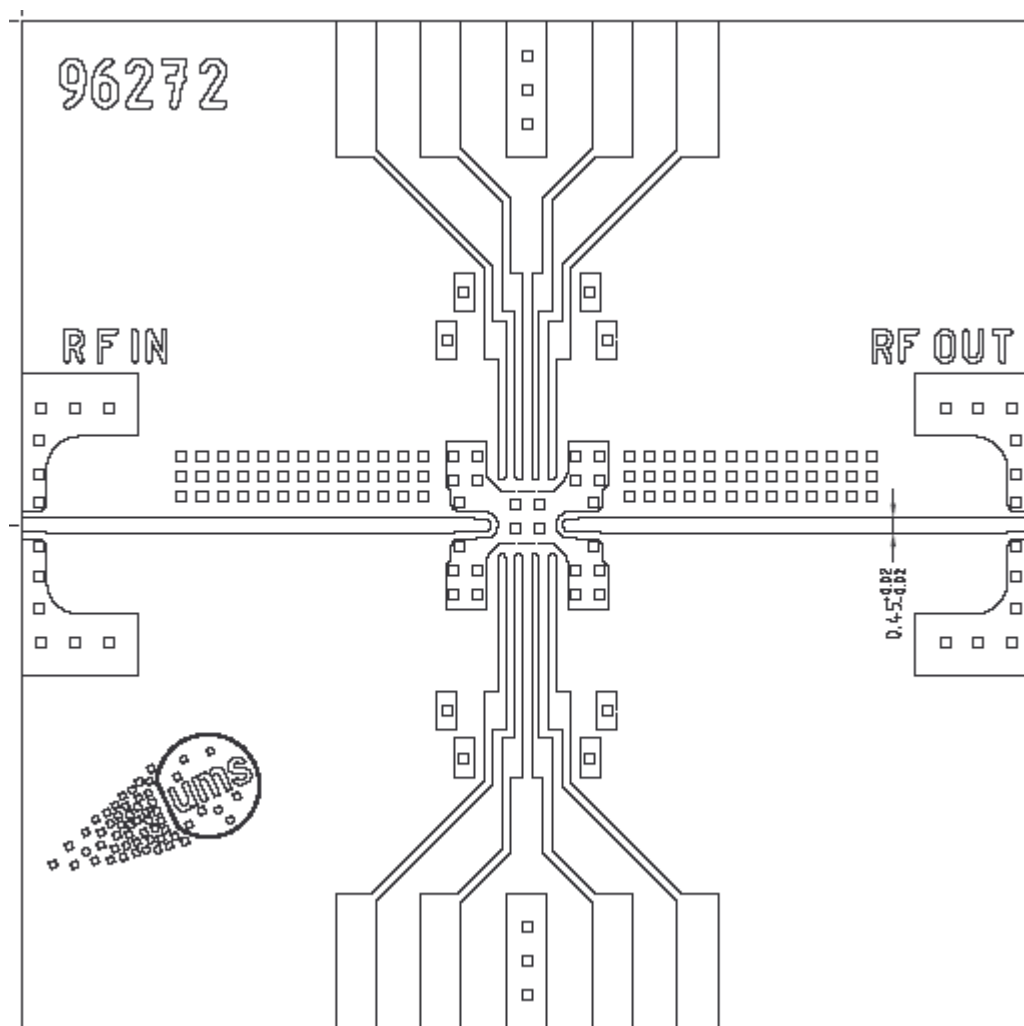
## SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

**Proposed Assembly board "96272" for the 16L-QFN3x3 products characterization.**

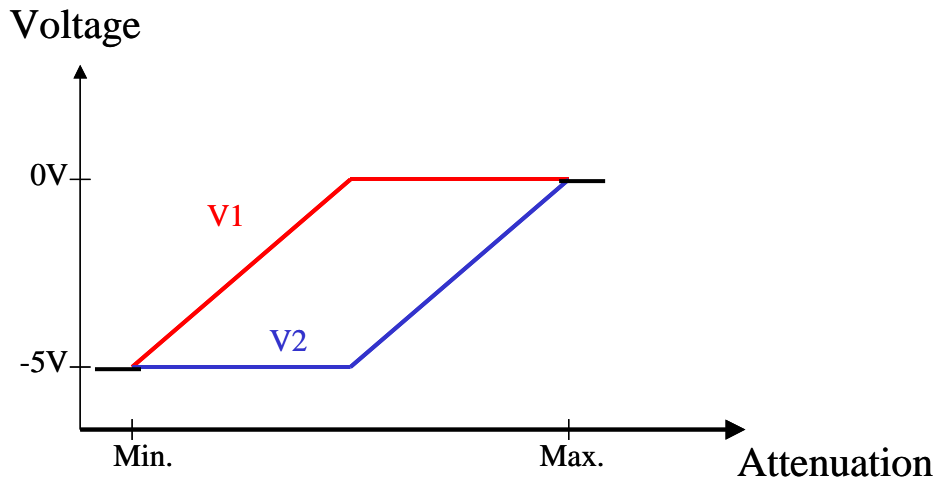
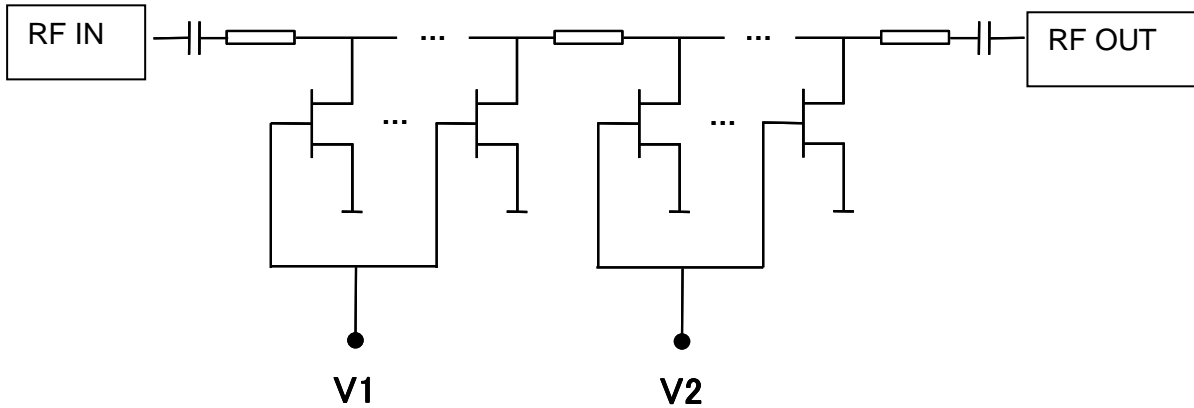
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



## Biasing sequence

To obtain good performances in linearity, biasing voltage should be applied as following:

- Control of 1<sup>st</sup> stage attenuation with V1 from -5V to 0V, with V2 fixed at -5V
- Control of 2<sup>nd</sup> stage with V2 from -5V to 0V, with V1 fixed at 0V



## Ordering Information

QFN 3x3 RoHS compliant package: CHT4690-QAG/XY  
 Stick: XY = 20      Tape & reel: XY = 21

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