United Monolithic Semiconductors

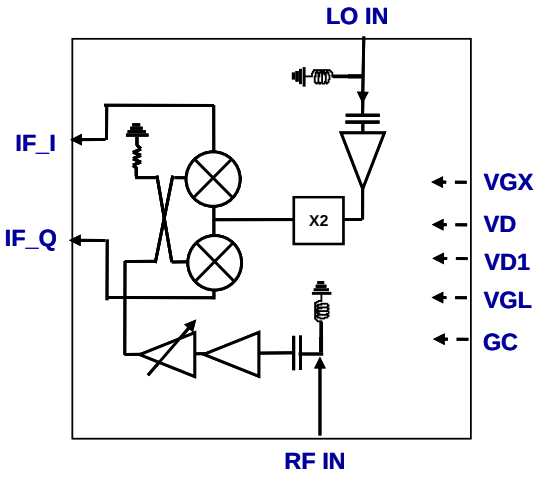
CHR3894-98F

37-40GHz Integrated Down Converter

GaAs Monolithic Microwave IC

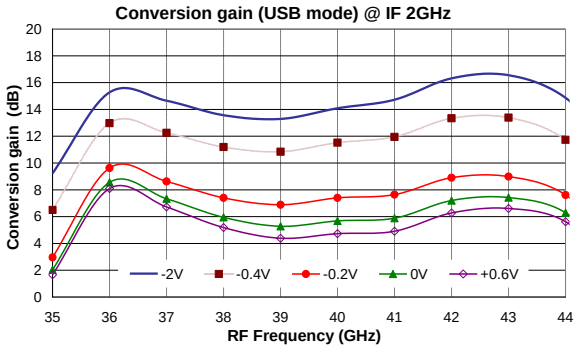
Description

The CHR3894-98F is a multifunction monolithic receiver, which integrates a balanced cold fet mixer, a LO chain with buffers associated to a time two multiplier, and a RF low noise amplifier including gain control.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performances: 37-40GHz
- 13dB Conversion gain
- 16dBc Image Rejection
- 2dBm IIP3 without attenuation (GC=-2V)
- 8dB Gain Control range
- 4.5dB Noise Figure for IF>0.1GHz
- 0dBm LO input Power
- DC bias: Vd=4V @ Id=250mA
- Chip size 2.6x2.7x0.1mm



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40	GHz
F_{OL}	LO frequency range	17.5		21.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain without attenuation		13		dB

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Main Characteristics

Tamb.= +25°C, VD = VD1 = +4V (1)

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40	GHz
F_{OL}	LO frequency range	17.5		21.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain without attenuation (2)		13		dB
ΔG	Gain Control range		8		dB
NF	Noise Figure without attenuation, for IF>0.1GHz		4.5		dB
Im_rej	Image rejection (2)		16		dBc
P_{Lo}	LO input power		0		dBm
IIP3	Input IP3 without attenuation		2		dBm
IIP3	Input IP3 @ all attenuation		0		dBm
LO RL	Input LO Return Loss		-12		dB
RF RL	Input RF Return Loss		-8		dB
LO/RF iso	Isolation LO on RF @ LO		-40		dBm
2LO/RF iso	Isolation LO on RF @ 2LO		-30		dBm
VGL	LNA DC gate voltage		-0.15		V
GC	Gain Control DC voltage	-2		0.6	V
VGX	Multiplier DC gate voltage		-0.9		V
IDt	Total drain current (ID+ID1) (3)		250		mA

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.
A bonding wire of typically 0.1 to 0.25nH will improve the matching at the accesses.

(1) VD: LO-chain drain bias voltage.
VD1: LNA drain bias voltage.

(2) An external combiner 90° is required on I / Q.

(3) ID: LO-chain drain current around 125mA.
ID1: LNA drain current around 125mA, could be tuned with VGL.

Note: IDt is not affected by GC.

Electrostatic discharge sensitive device observe handling precautions!

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD, VD1	Drain bias voltage	4.5V	V
IDt	Drain bias current	340	mA
VGL, VGX	Gate bias voltage	-2 to +0.4	V
GC	Gain Control voltage	-2.5 to +0.8	V
P_RF	Maximum peak input power overdrive (2)	+15	dBm
P_LO	Maximum LO input power	+15	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD, VD1	DC drain voltages	4	V
ID1	LNA drain current controlled with VGL	125	mA
VGL	LNA DC gate voltage	-0.15	V
VGX	Multiplier DC gate voltage	-0.9	V
GC	Gain Control DC voltage	-2 to 0.6	V

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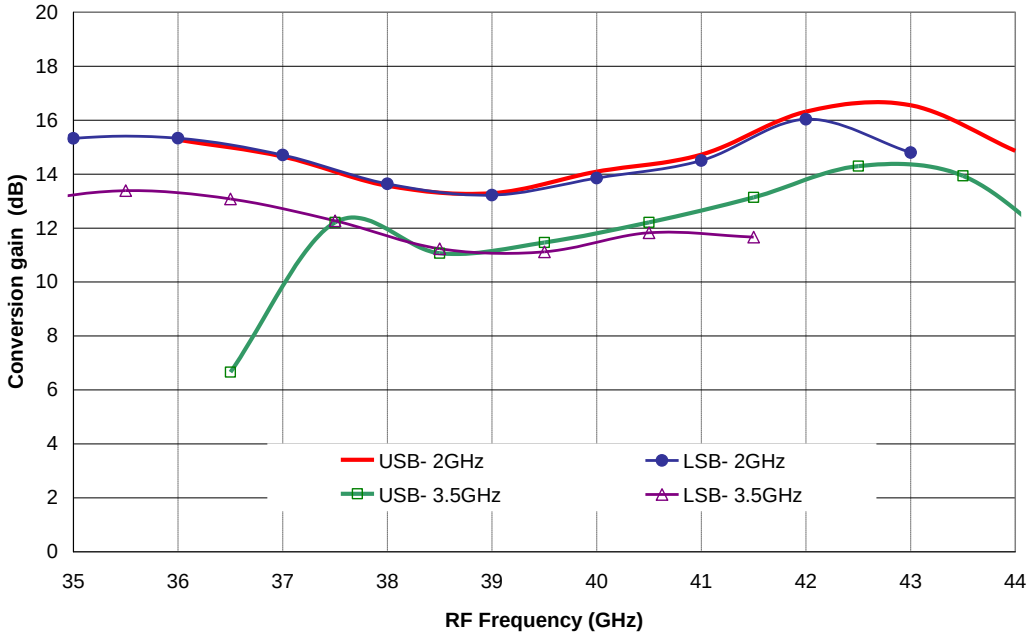
Typical Measured Performances

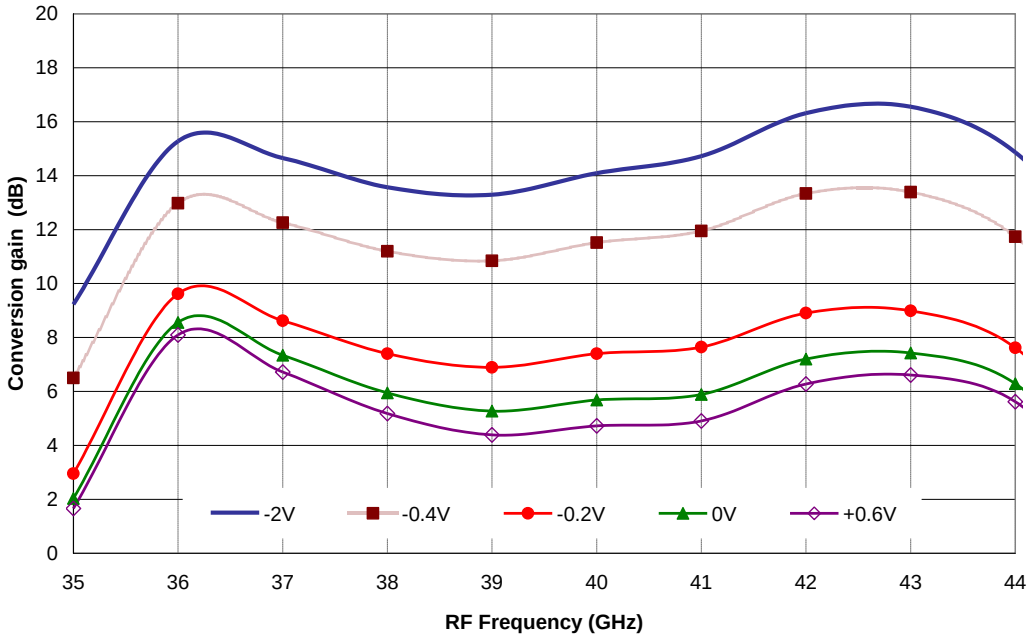
Tamb.= +25°C, VD = VD1 =+4V, VGL = -0.15V, VGX= -0.9V, P_LO = 0dBm (IDt = 250mA)

These values are representative of de-embedded onboard measurements as defined on the paragraph ”Evaluation mother board”.

Conversion Gain versus RF & IF frequency (USB & LSB modes) without attenuation: GC= -2V



Conversion Gain versus RF frequency and gain control voltage (IF 2GHz, USB mode)



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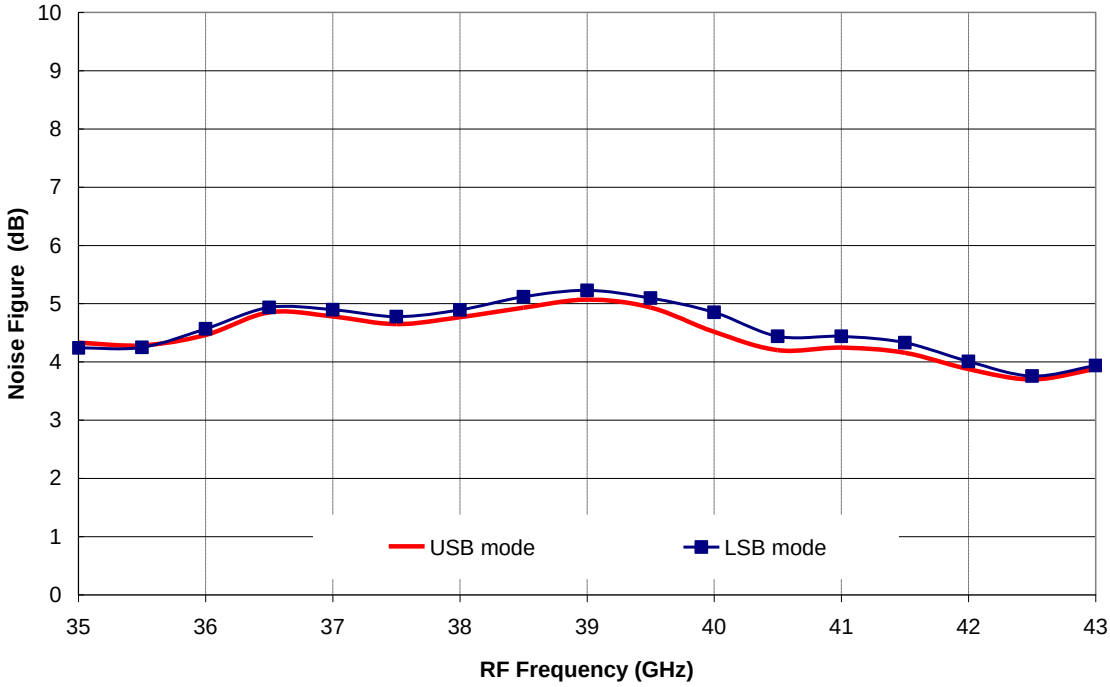
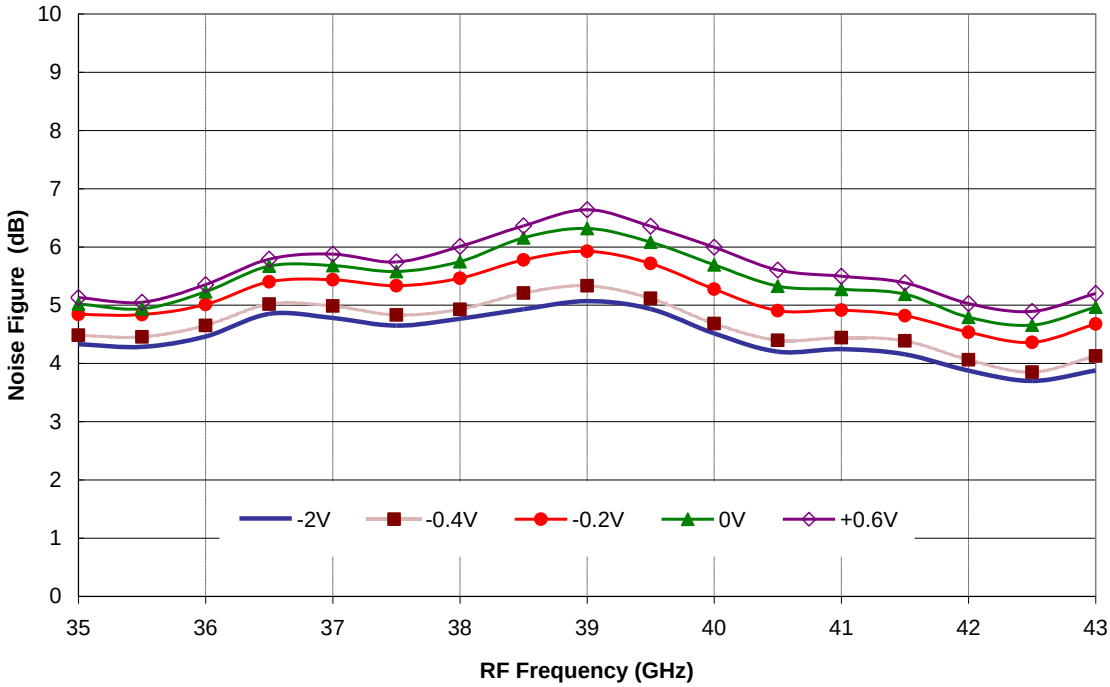
Typical Measured Performances

Tamb.= +25°C, VD = VD1 =+4V, VGL = -0.15V, VGX= -0.9V, P_LO = 0dBm (IDt = 250mA)

Noise figure versus RF frequency at IF 2GHz (USB & LSB modes) without attenuation: GC= -2V



Noise figure versus RF frequency and gain control voltage (IF 2GHz, USB mode)



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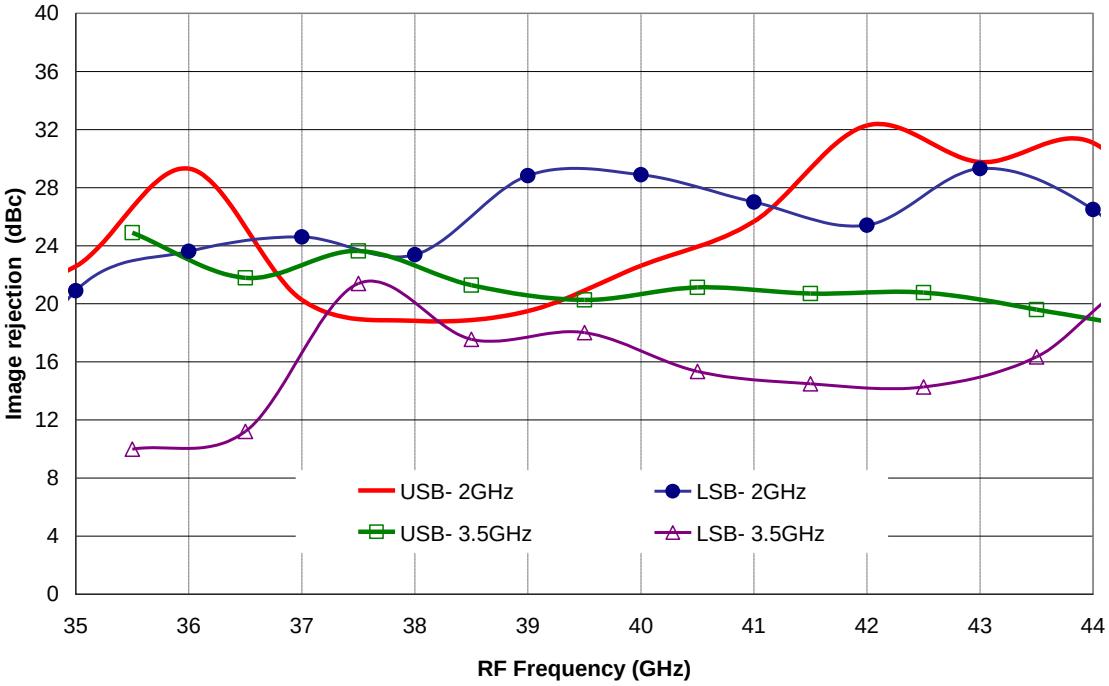
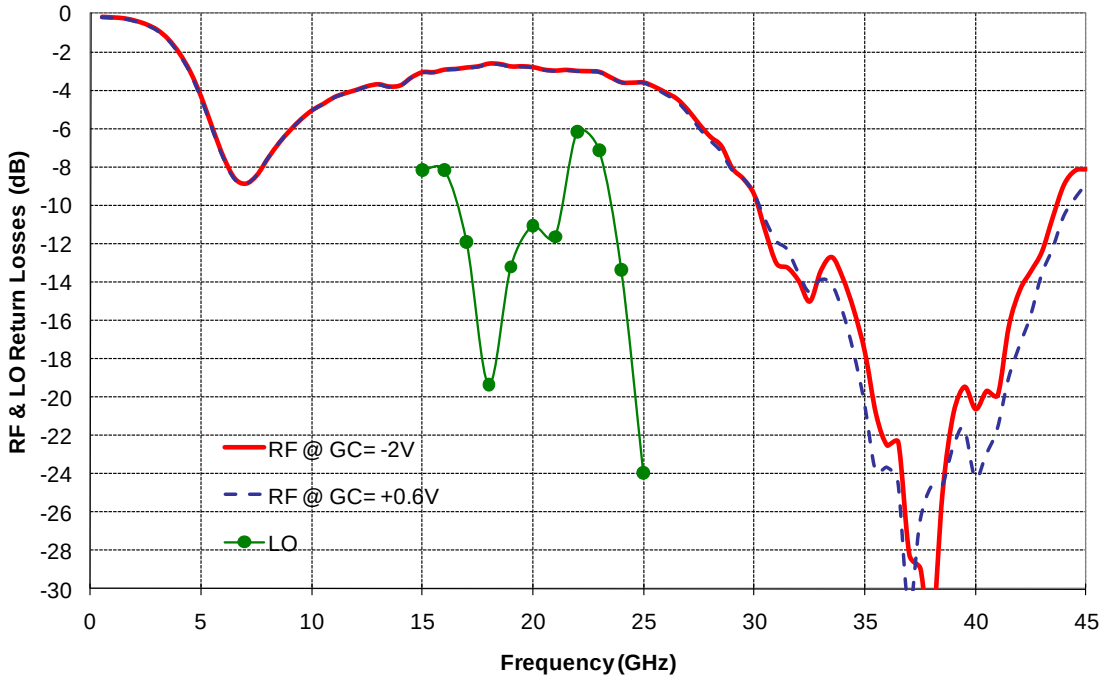
Typical Measured Performances

Tamb.= +25°C, VD = VD1 =+4V, VGL = -0.15V, VGX= -0.9V, P_LO = 0dBm (IDt = 250mA)

Image rejection versus RF & IF frequency (USB & LSB modes) without attenuation: GC= -2V



Return Losses (RF & LO) versus frequency and gain control voltage



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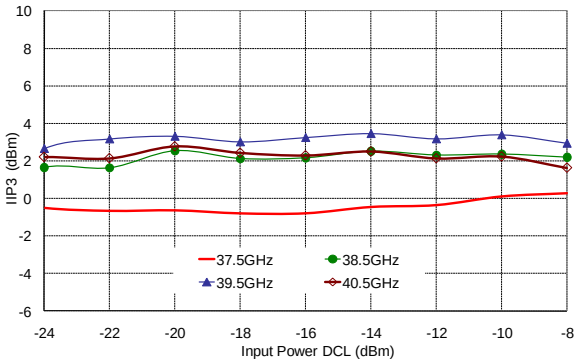
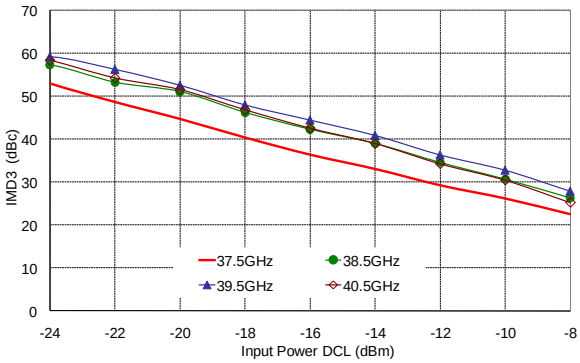
Typical Measured Performances

Tamb.= +25°C, VD = VD1 =+4V, VGL = -0.15V, VGX= -0.9V, P_LO = 0dBm (IDt = 250mA)

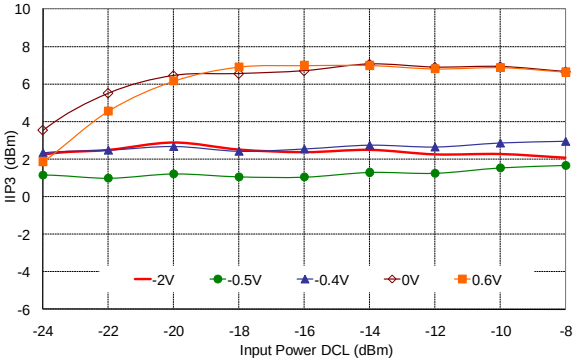
Input IP3 vs RF frequency at IF 3.5GHz without attenuation: GC= -2V



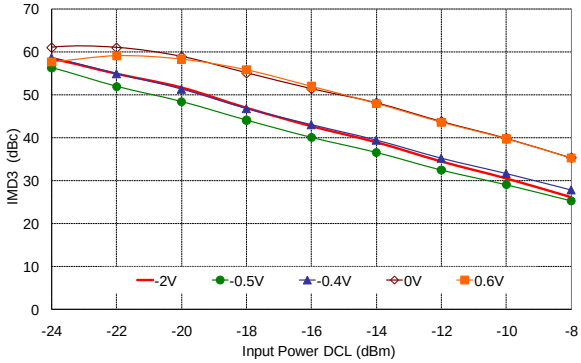
IMD3 vs RF frequency at IF 3.5GHz without attenuation: GC= -2V



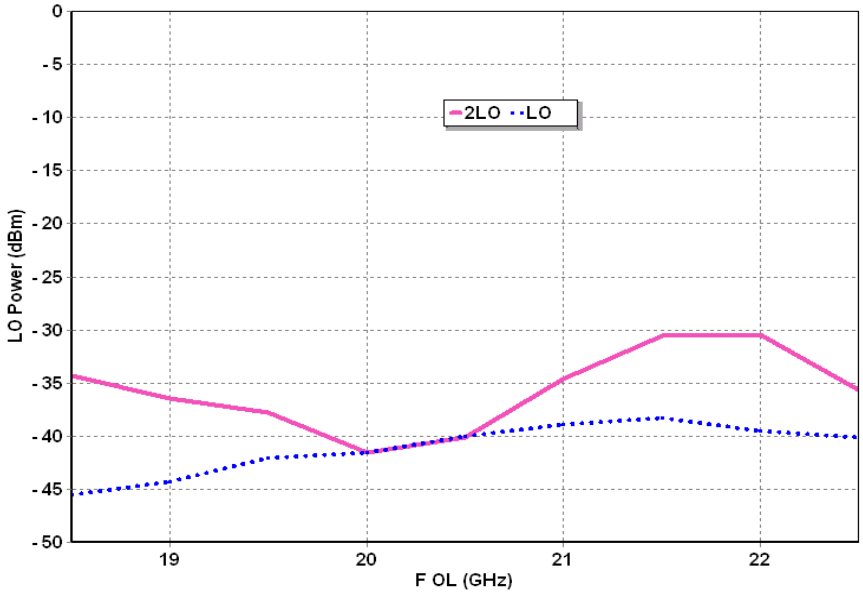
Input IP3 vs gain control voltage at 38GHz (IF 2GHz)



IMD3 vs gain control voltage at 38GHz (IF 2GHz)



Isolation LO on RF @ LO and 2LO



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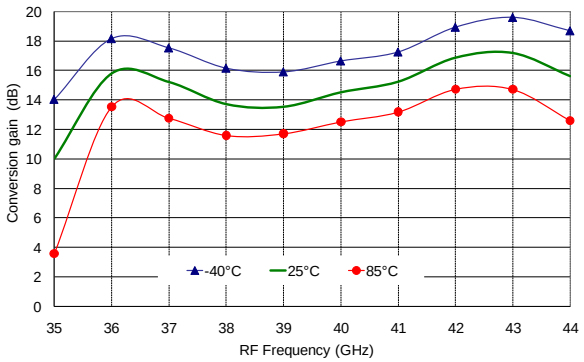
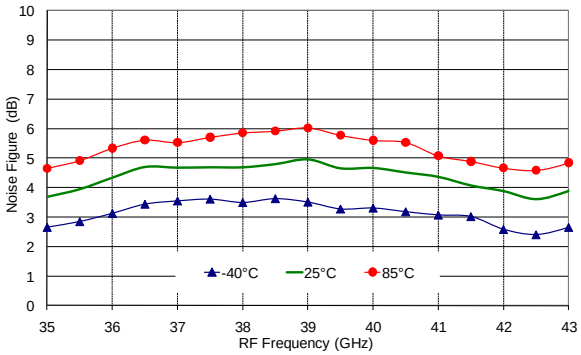
Typical Measured Performances versus Temperature

Tamb = +25°C, Tcold = -40°C, Thot = +85°C
VD = VD1 =+4V, VGL = -0.15V, VGX= -0.9V, P_LO = 0dBm

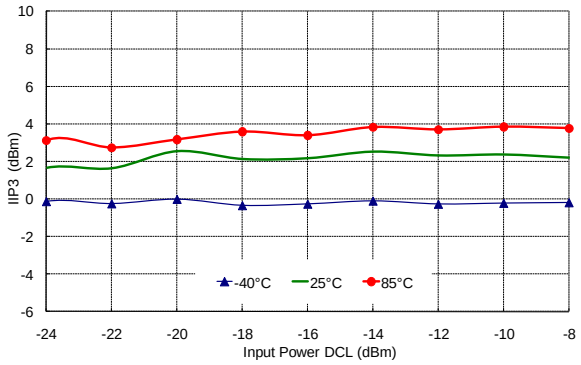
Conversion Gain versus temperature
IF 2GHz, USB mode
without attenuation: GC= -2V



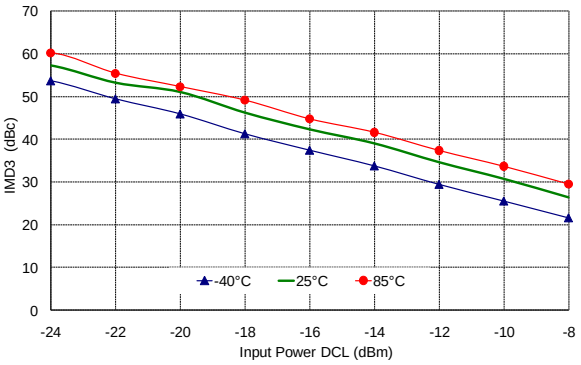
Noise figure versus temperature
IF 2GHz, USB mode
without attenuation: GC= -2V



Input IP3 vs temperature
at 38.5GHz (IF 3.5GHz)
without attenuation: GC= -2V



IMD3 vs temperature
at 38.5GHz (IF 3.5GHz)
without attenuation: GC= -2V



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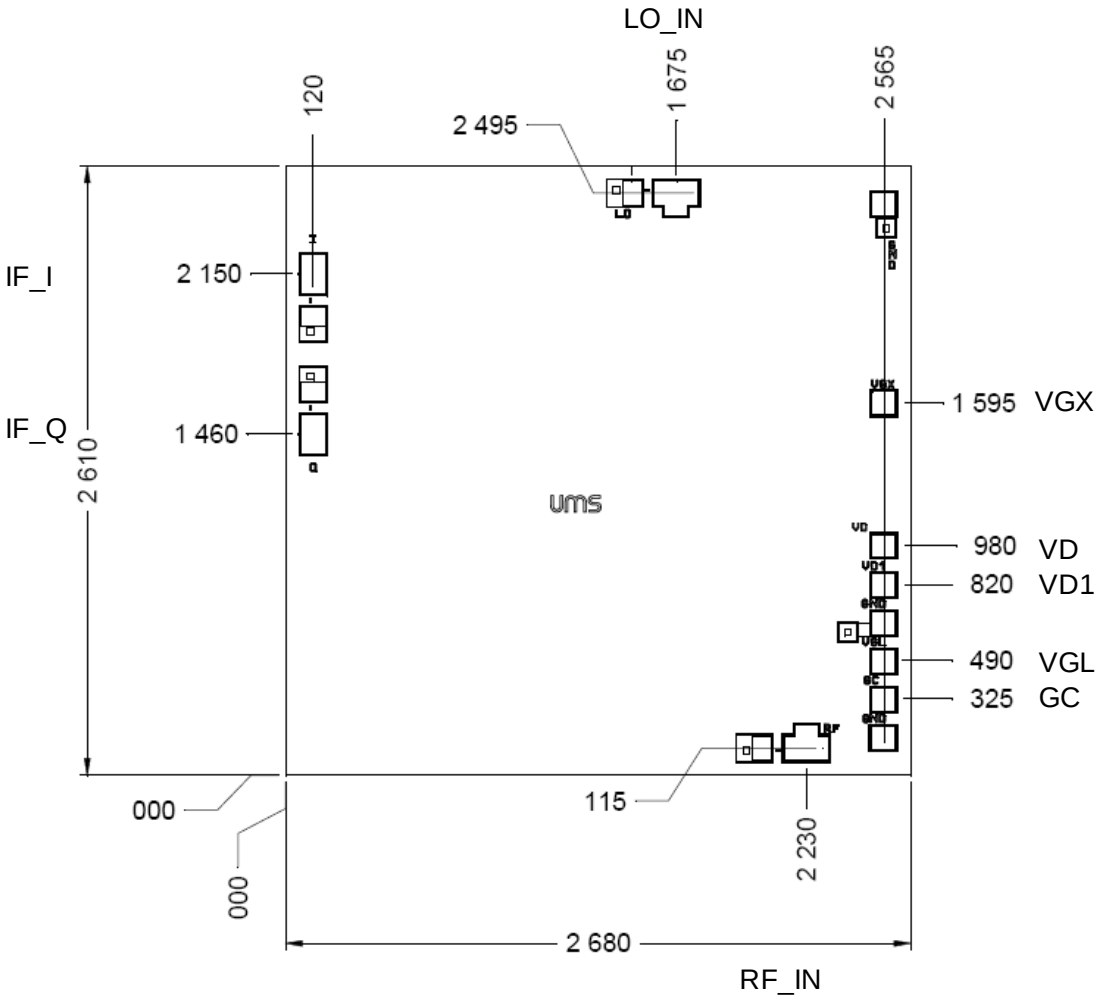
Mechanical data



Chip thickness: 100µm.
Chip size: 2680 X2610µm ±35µm
All dimensions are in micrometers

It is strongly recommended to add capacitor typically 120pF on each DC access (VGX, VD, VD1, VGL and GC).
VD & VD1 could be connected together on the same capacitor. VD1 is the LNA drain access.

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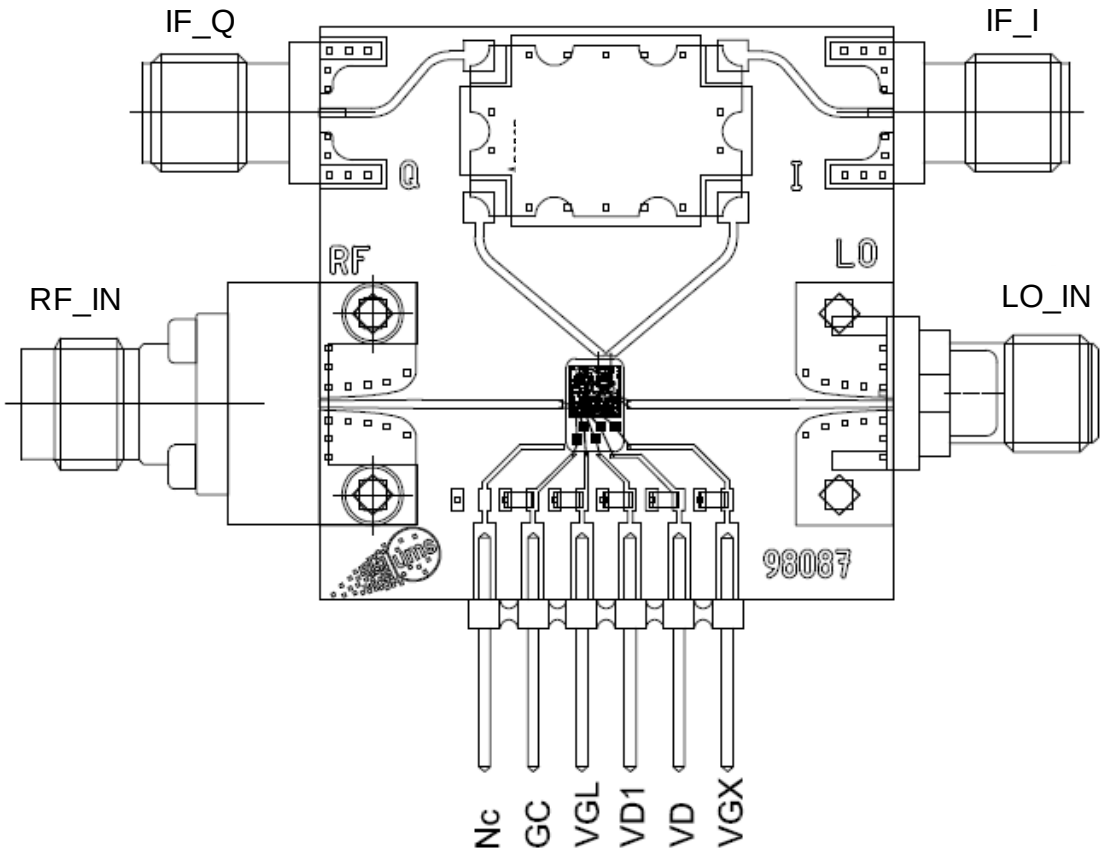
Evaluation mother board

- Based on typically Ro4003 / 8mils or equivalent.
- Decoupling capacitors of 120nF and 10nF ±10% are recommended for all DC accesses.
- Hybrid coupler 90°: 2-4GHz.
- The board losses are estimated from 2 to 3dB in the frequency range.



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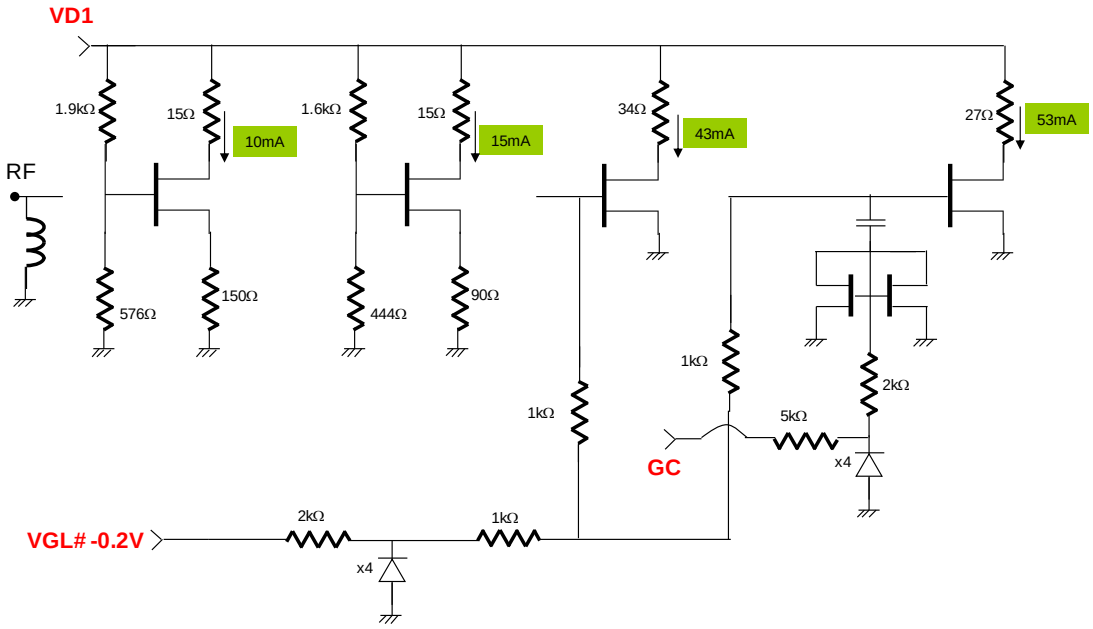
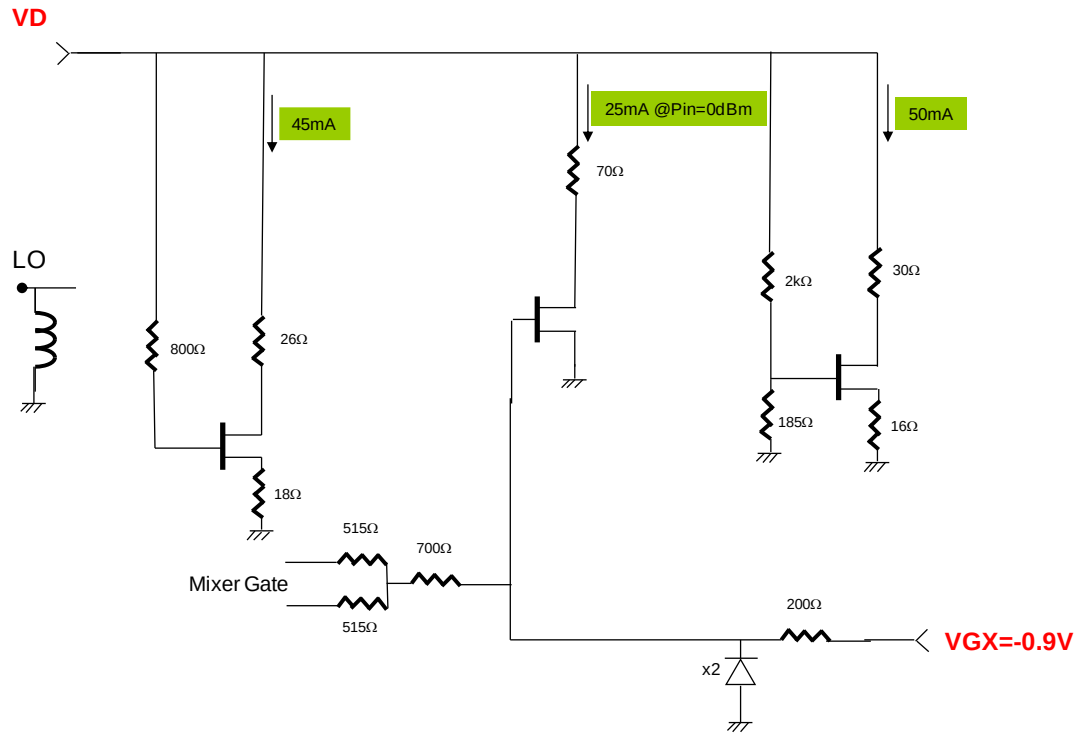
DC Schematic

LNA: 4V, 125mA



LO chain: 4V, 125mA



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Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.
ESD protections are also implemented on gate and control accesses (Vgx, Vgl and GC).

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form:	CHR3894-98F/00

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