

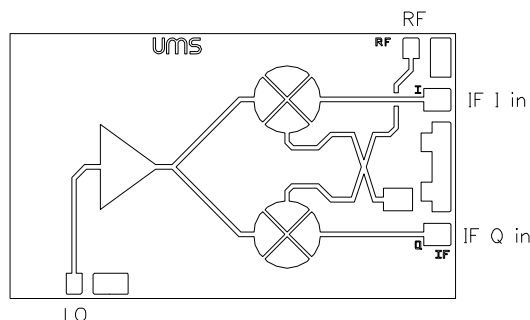
25-32GHz Single Side Band Mixer

GaAs Monolithic Microwave IC

Description

The CHM1291-99F is a multifunction chip (MFC) which integrates a LO buffer amplifier and a sub-harmonically balanced diodes mixer for 2LO suppression and image rejection. It is usable both for up-conversion and down-conversion. It is designed for a wide range of applications, typically commercial communication systems for broadband local access (LMDS). The backside of the chip is both RF and DC grounded. This helps simplify the assembly process.

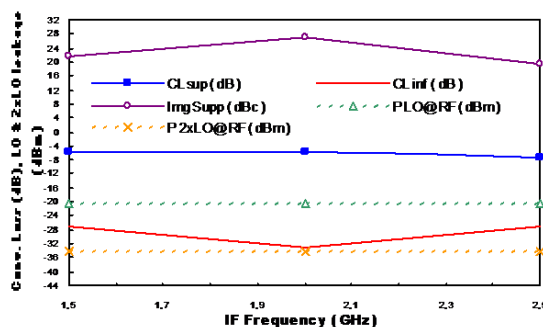
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



Main Features

- Broadband performance : 25-32GHz
- 11dB conversion Loss
- 15dBc image rejection
- +5dBm LO input power
- +1dBm input power (1dB gain comp.)
- Low DC power consumption, 55mA@3.5V
- Chip size : 2.06 x 1.25 x 0.10mm

Up-Conversion supradyn mode with external combiner
P_{LO}=+5dBm F_{LO}=14GHz



T_{amb}=+25°C

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	25		32	GHz
F _{LO}	LO frequency range	12		15.5	GHz
F _{IF}	IF frequency range	0.1		3	GHz
L _c	Conversion Loss		11	15	dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics for Broadband OperationT_{amb}=+25°C, V_d=3.5V, I_d=55mA

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	25		32	GHz
F _{LO}	LO frequency range	12		15.5	GHz
F _{IF}	IF frequency range	0.1		3	GHz
L _c	Conversion Loss		11	15	dB
P _{LO}	LO Input power		+5		dBm
2xLO Leak	2xLO Leakage (for P _{LO} =+5dBm)		-35	-30	dBm
Img Rej	Image Rejection (1)	13	15		dBc
P1dB	Input power at 1dB gain compression	-2	0		dBm
P03	Input power at 3dB gain compression	0	+2		dBm
IP3	Input 3 rd order intercept point		+8		dBm
LO Match	LO VSWR (2)		2.0:1		
RF Match	RF VSWR (2)		2.0:1		
IF Match	IF VSWR (2)		2.0:1		
I _d	Bias current		55		mA

(1) With external quadrature hybrid coupler (reference on request). The minimal value depends on the quality of the external quadrature combiner.

(2) A bonding wire of typically 0.1 to 0.15nH will improve the accesses matching.

Current source biasing network is recommended.

Absolute Maximum RatingsT_{amb}=+25°C (1)

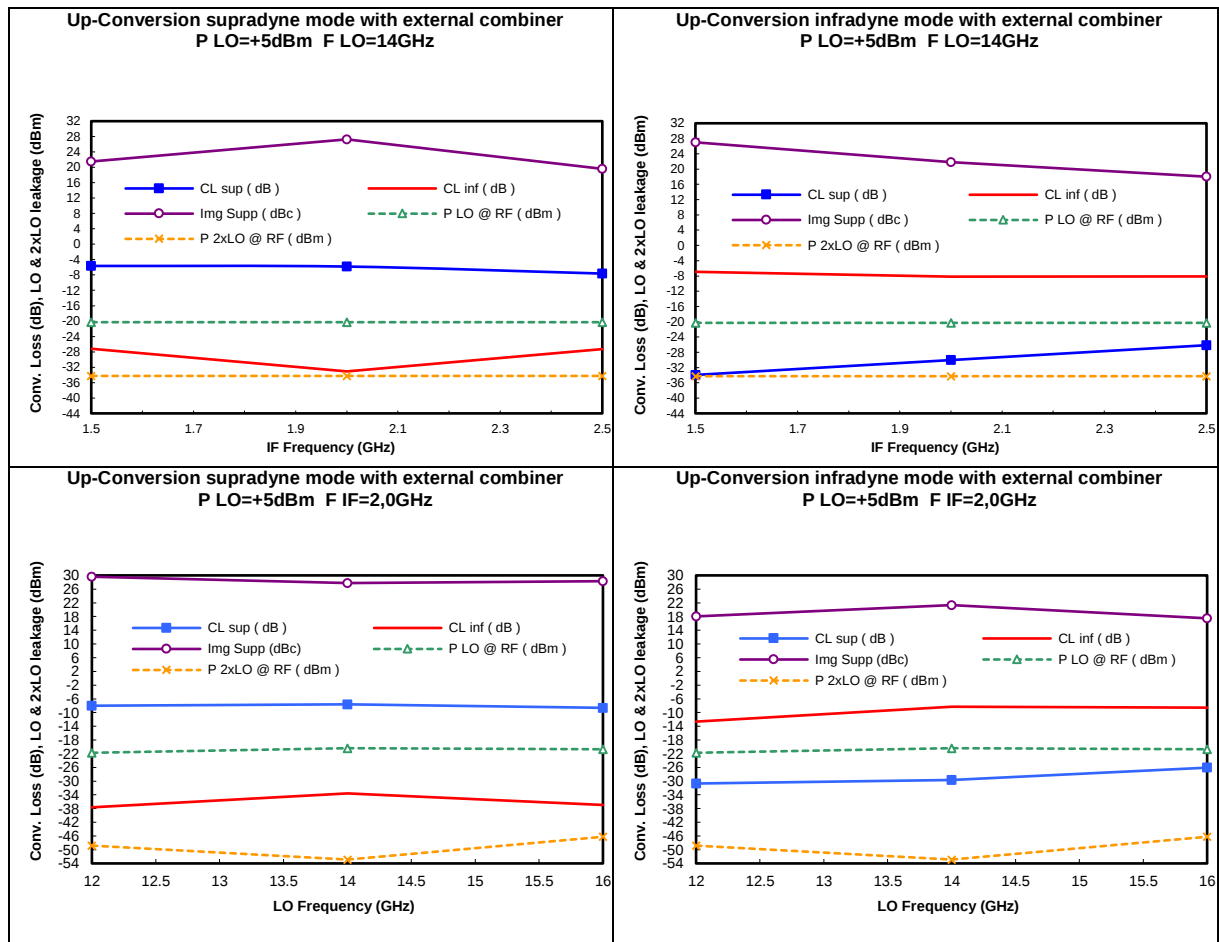
Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	4.0	V
I _d	Drain bias current	100	mA
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

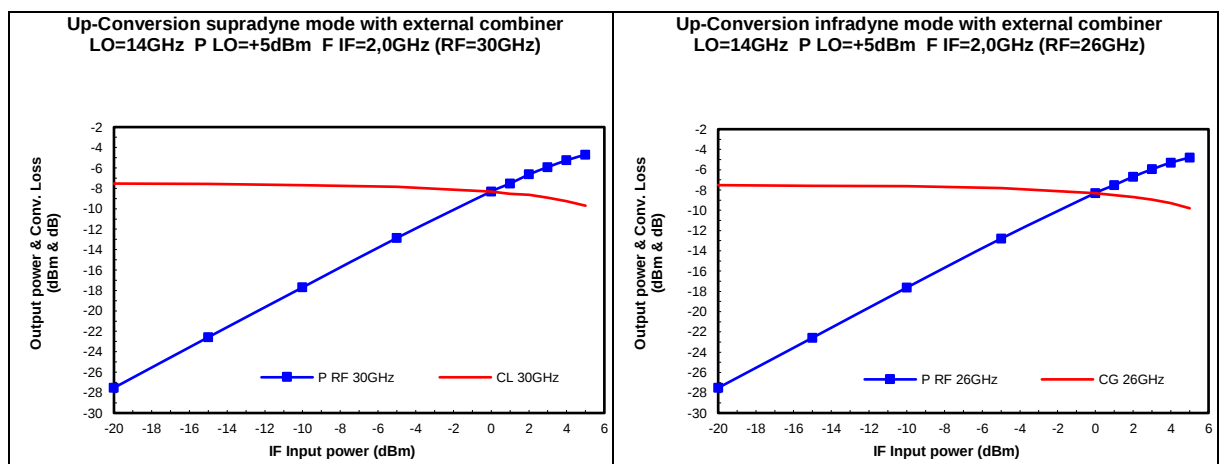
Typical On-wafer Measurements in Up-Conversion mode with external IF quadrature combiner

Bias conditions: $T_{amb}=+25^{\circ}\text{C}$, $V_d=3.5\text{V}$, $I_d=55\text{mA}$



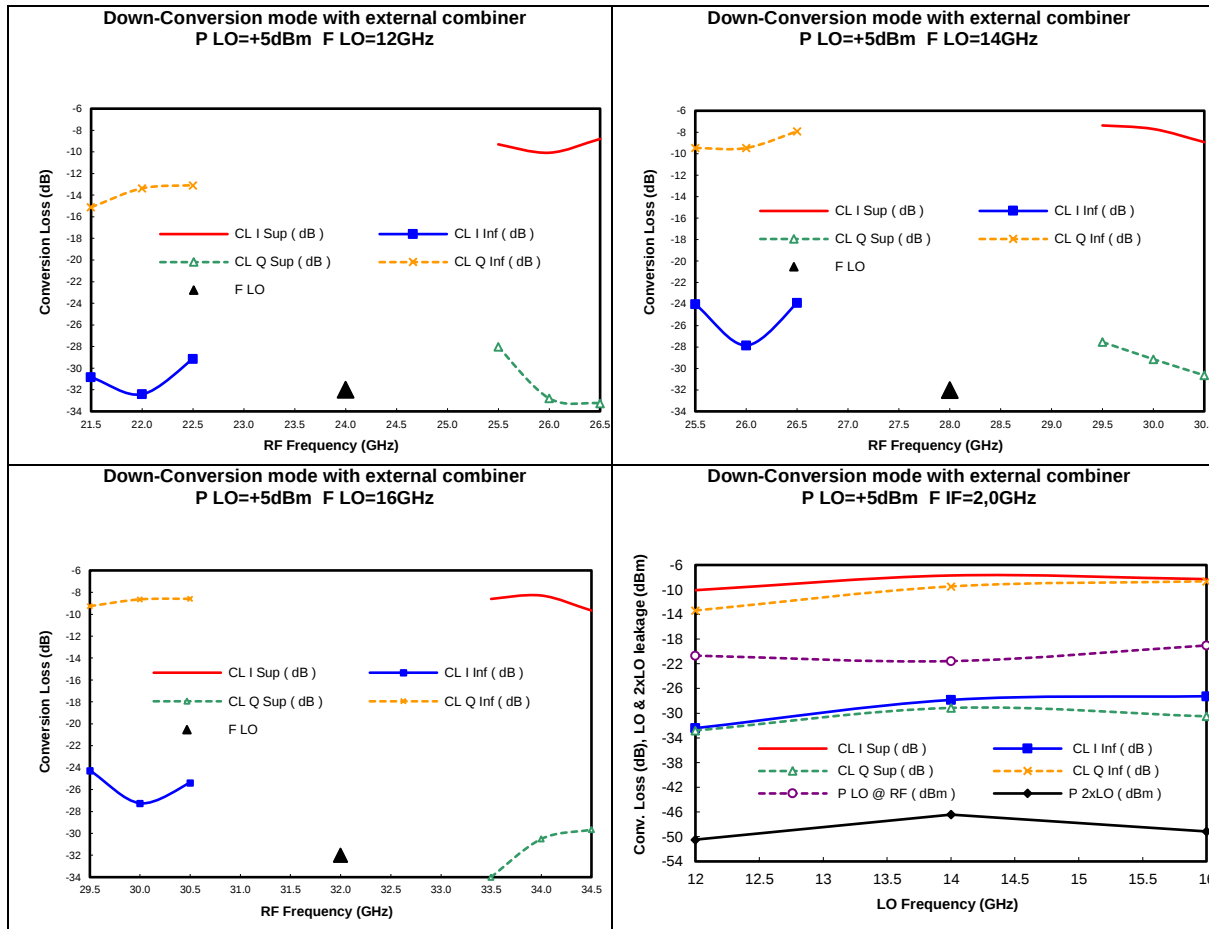
Typical On-wafer Compression Measurements in Up-Conversion mode with external IF quadrature combiner

Bias conditions: $T_{amb}=+25^{\circ}\text{C}$, $V_d=3.5\text{V}$, $I_d=55\text{mA}$



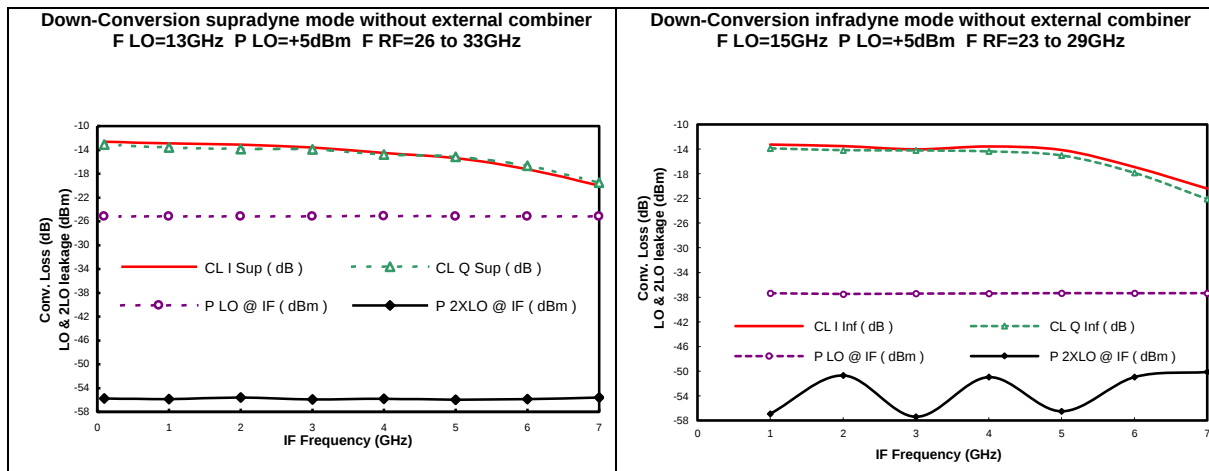
Typical On-wafer Measurements in Down-Conversion mode with external IF quadrature combiner

Bias conditions: Tamb=+25°C, Vd=3.5V, Id=55mA

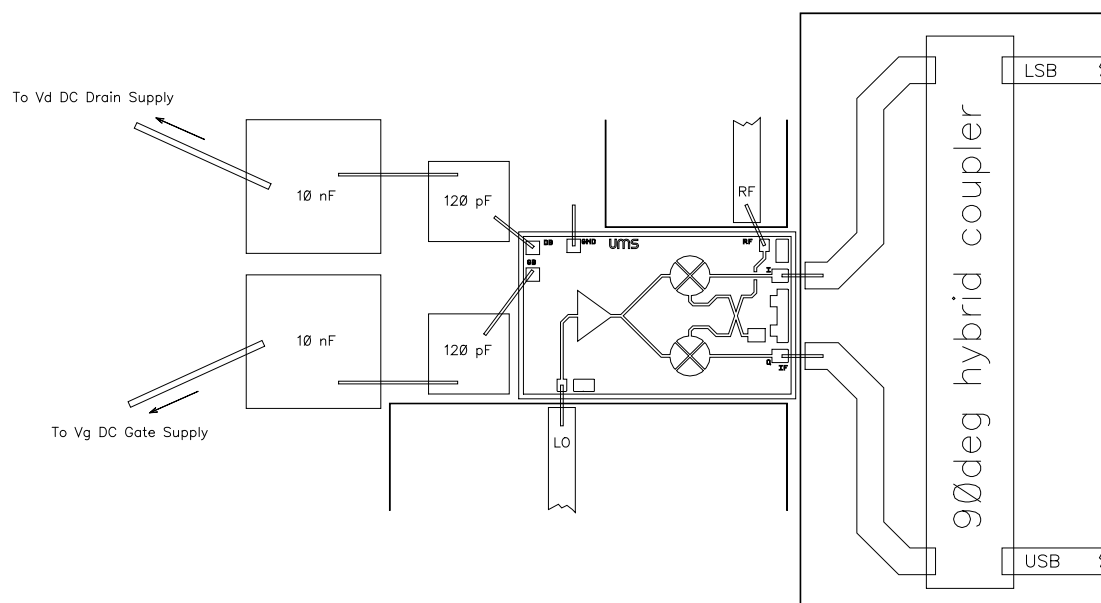


Typical On-wafer Measurements in Down-Conversion mode without external IF quadrature combiner

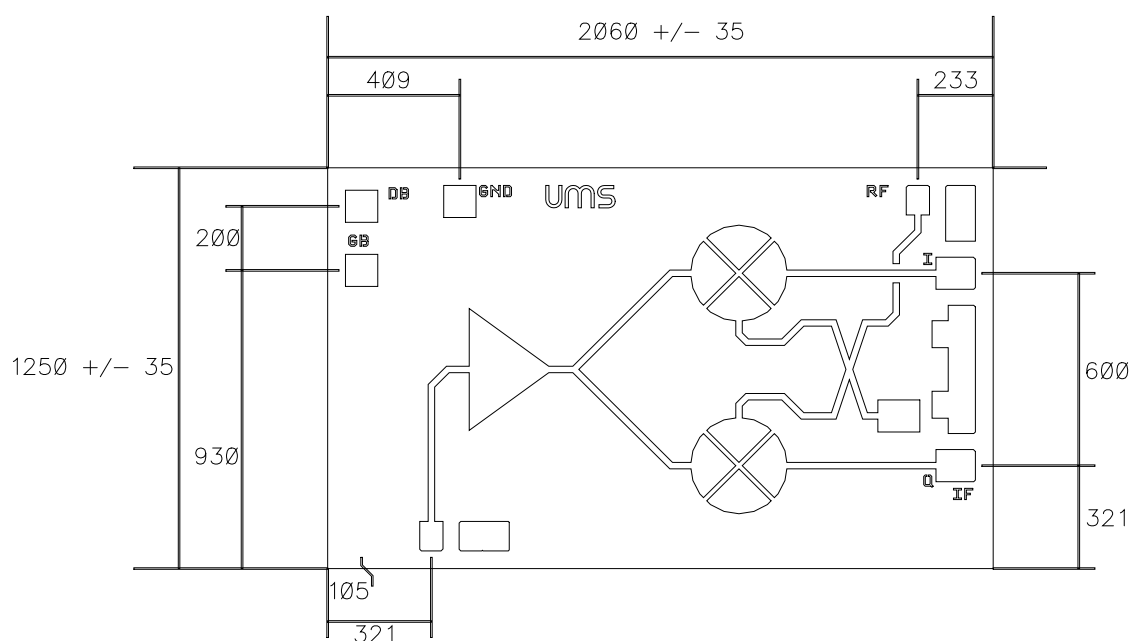
Bias conditions: Tamb=+25°C, Vd=3.5V, Id=55mA



Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



Bonding pad positions
(Chip thickness : 100µm. All dimensions are in micrometers)

Ordering Information

Chip form : CHM1291-99F/00

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