

## 140W Power Bar GaN HEMT on SiC

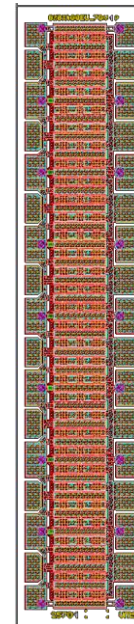
### Description

The CHKA012a99F is a 140W Gallium Nitride High Electron Mobility Transistor.

This product offers a general purpose and broadband solution for a variety of RF power applications such as radar and telecommunication.

It is developed on a 0.5 $\mu$ m gate length GaN HEMT technology on SiC substrate and is compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006

It is proposed in a bare die form and requires an external matching circuitry.



### Main Features

- Wide band capability up to 4GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias:  $V_{DS}$  up to 50V
- Chip size: 1x4.84x0.1mm
- RoHS N°2011/65
- REACH N°1907/2006

### Main Electrical Characteristics

$T_{ref} = +25^{\circ}C$ , CW mode, Freq = 3GHz,  $V_{DS} = 50V$ ,  $I_{D-Q} = 640mA$

Symbol	Parameter	Min	Typ	Max	Unit
$G_{SS}$	Small Signal Gain		19		dB
$P_{SAT}$	Saturated Output Power		140		W
$P_{AE}$	Max Power Added Efficiency		76		%
$G_{PAE\_MAX}$	Associated Gain at Max PAE		14		dB

These values are deduced from elementary power cell performances

## Recommended Operating Ratings (ROR)

$T_{ref} = +25^{\circ}\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{DS}$	Drain to Source Voltage			50	V	
$V_{GS}$	Gate to Source Voltage		-1.9		V	$V_{DS}=50\text{V}$ , $I_{D\_Q}=640\text{mA}$
$I_{D\_Q}$	Quiescent Drain Current		0.64	2.05	A	$V_{DS}=50\text{V}$
$I_{D\_MAX}$	Drain Current		4.1	<sup>(1)</sup>	A	$V_{DS}=50\text{V}$ , compressed mode
$I_{G\_MAX}$	Gate Current in forward mode		0	100	mA	DC or Compressed mode
$T_{j\_MAX}$	Junction temperature			200	$^{\circ}\text{C}$	<sup>(1)</sup>

<sup>(1)</sup> Power dissipation and  $T_{ref}$  (back side temperature) must be considered

## DC Characteristics

$T_{ref} = +25^{\circ}\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_P$	Pinch-Off Voltage	-2.7	-2	-1.5	V	$V_{DS}=10\text{V}$ , $I_{DS} = I_{DSS} / 100$
$I_{D\_SAT}$	Saturated Drain Current		15.4		A	<sup>(1)</sup> , $V_{DS}=10\text{V}$ , $V_{GS}=1\text{V}$
$I_{G\_leak}$	Gate Leakage Current	-2.6			mA	$V_{DS}=50\text{V}$ , $V_{GS}=-7\text{V}$
$V_{BDS}$	Drain-Source Breakdown Voltage		180		V	$V_{GS}=-7\text{V}$ , $I_{DS}=20\text{mA}$

<sup>(1)</sup> For information, limited by  $I_{D\_MAX}$  and  $T_{j\_MAX}$ , see on ROR & AMR

## RF Characteristics

$T_{ref} = +25^{\circ}\text{C}$ , CW mode, Freq = 3GHz,  $V_{DS} = 50\text{V}$ ,  $I_{D\_Q} = 640\text{mA}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$G_{SS}$	Small Signal Gain		19		dB	
$P_{SAT}$	Saturated Output Power		140		W	
$P_{AE}$	Max Power Added Efficiency		76		%	
$G_{PAE\_MAX}$	Associated Gain at Max PAE		14		dB	

These values are deduced from elementary power cell performances.

## Absolute Maximum Ratings (AMR)

T<sub>ref</sub> = +25°C <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

Symbol	Parameter	Rating	Unit	Note
V <sub>DS_Q</sub>	Drain-Source Biasing Voltage	60	V	
V <sub>GS_Q</sub>	Gate-Source Biasing Voltage	-10, +2	V	(4), (5)
I <sub>G_MAX</sub>	Maximum Gate Current in forward mode	200	mA	
I <sub>G_MIN</sub>	Maximum Gate Current in reverse mode	-13	mA	
I <sub>D_MAX</sub>	Maximum Drain Current	See note		(4)
P <sub>IN</sub>	Maximum Input Power	See note		(5)
T <sub>j_MAX</sub>	Maximum Junction Temperature	230	°C	
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C	
T <sub>ref</sub>	Back Side Operating Temperature	See note	°C	(4)

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

<sup>(2)</sup> Duration < 1s.

<sup>(3)</sup> The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

<sup>(4)</sup> T<sub>ref</sub> = back side temperature. Max junction temperature must be considered

<sup>(5)</sup> Linked to and limited by I<sub>G\_MAX</sub> & I<sub>G\_MIN</sub> values. Maximum input power depends on frequency and should not exceed 2dB above PAE<sub>max</sub>.

## Biasing procedure

1. Bias power bar gate voltage at V<sub>GS</sub> close to V<sub>p</sub> (Typically: V<sub>GS</sub> ≈ -5V)
2. Apply V<sub>DS</sub> bias voltage (Typically: V<sub>DS</sub> = 50V)
3. Increase V<sub>GS</sub> up to quiescent bias drain current I<sub>D\_Q</sub>

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.

A drain current control is recommended on the biasing network.

## Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature ( $T_j$ ). This temperature is defined as the peak temperature in the channel area.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHKA012a99F is fabricated (GaN Power HEMT 0.5 $\mu$ m).

The temperature  $T_b$  is defined as the chip back side temperature

The thermal resistance ( $R_{th}$ ) is given for the full power bar, in “equivalent” CW operating mode and in two different configurations as given in the table. The device assembly must be adapted to the operating mode. Thermal analysis is recommended. More information is available on request.

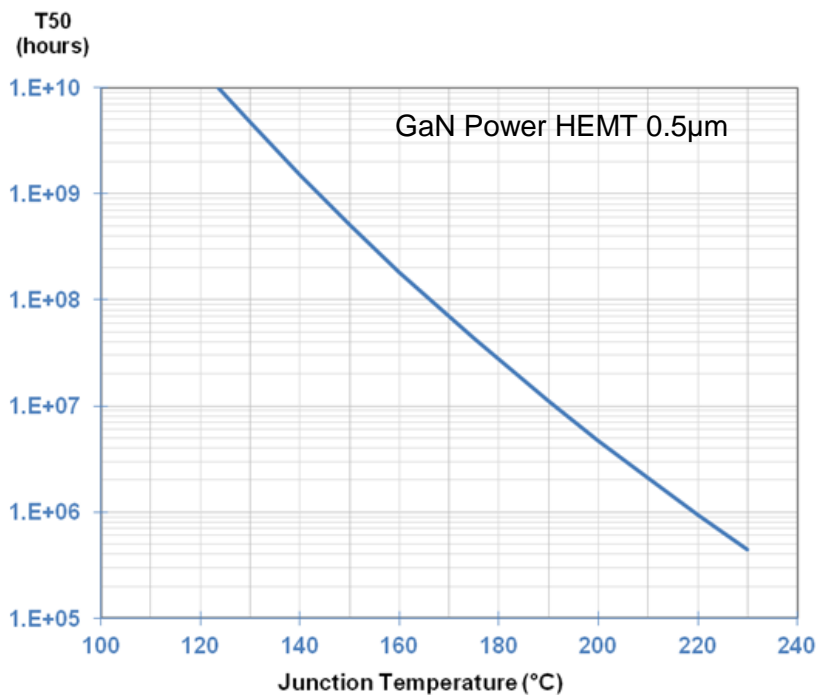
Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	$R_{th}$	Bare die characteristic $T_b = 100^\circ\text{C}$	0.55	$^\circ\text{C}/\text{W}$
Junction Temperature	$T_j$	$P_{diss} = 100\text{W}$ CW	155	$^\circ\text{C}$

The back side temperature ( $T_b$ ) is considered uniform on all the surface

Typical Thermal Resistance	$R_{th}$	Bare die on carrier characteristic $T_c = 85^\circ\text{C}$	1.2	$^\circ\text{C}/\text{W}$
Junction Temperature	$T_j$	$P_{diss} = 95\text{W}$ CW	200	$^\circ\text{C}$

The reference temperature ( $T_c$ ) is defined on the carrier back side. The power bar is mounted on carrier plate (20 $\mu$ m Au/Sn soldering + 1.5mm Cu/Mo/Cu).

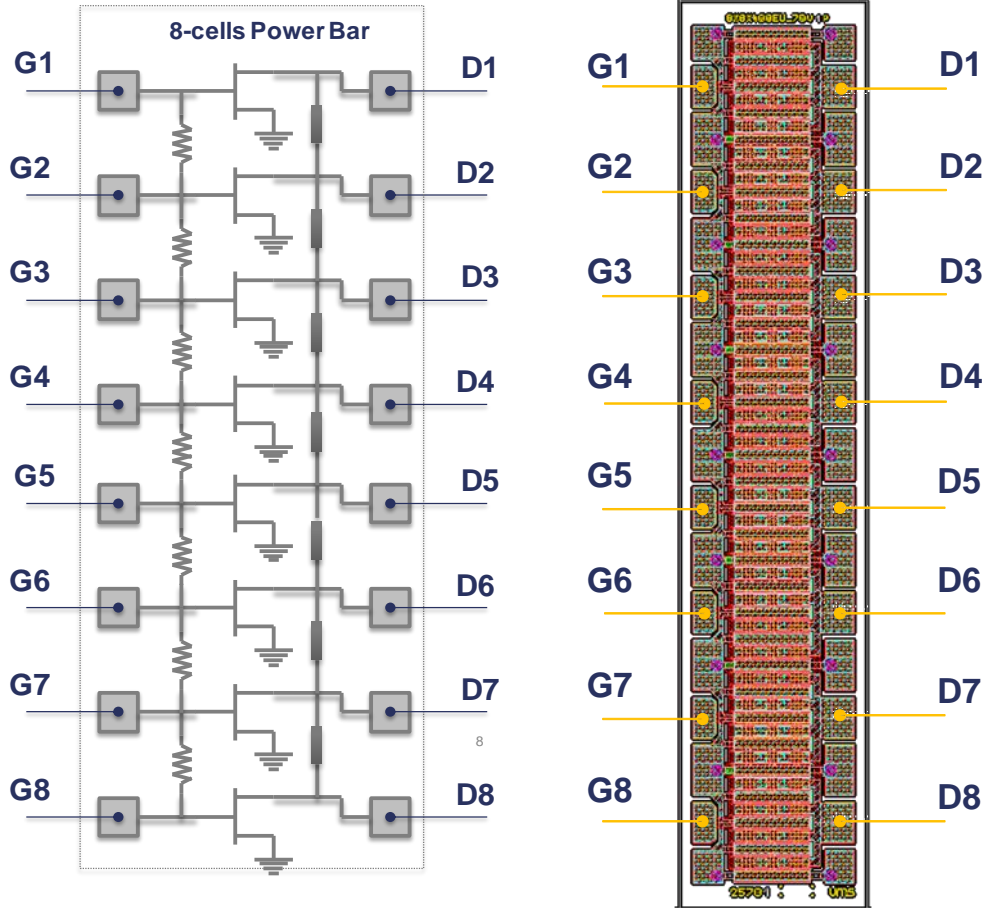
### Median Life Time versus Junction Temperature



**Power Bar Description**

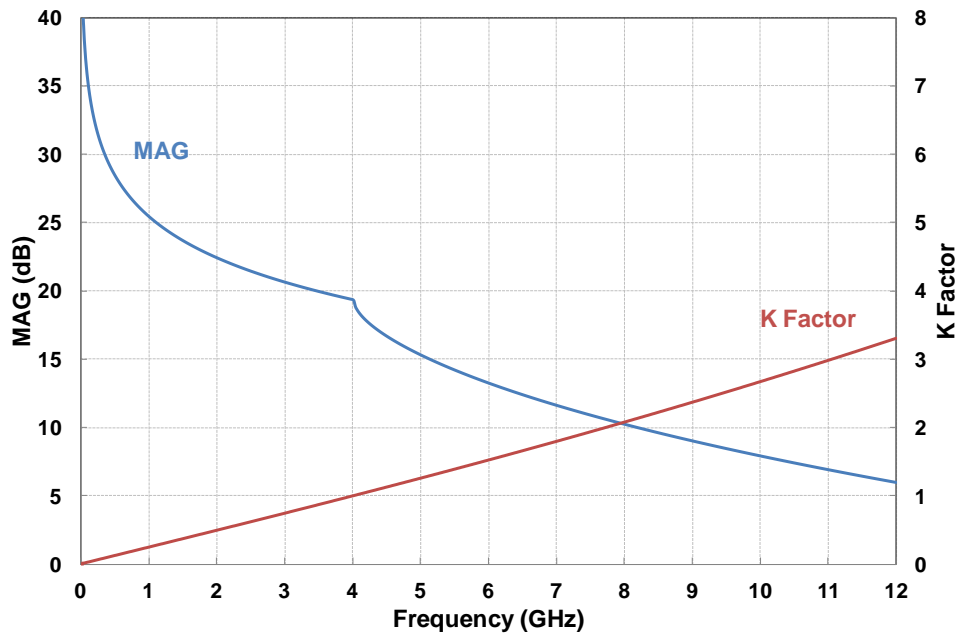
The CHKA012a99F is composed of 8 elementary 17W cells. These cells are connected together with a specific network providing a good compromise between performance and stability (resistance between gates and short circuit on drains). The reference planes are at the center of the bonding pads.

A multiport non-linear model is available on request.



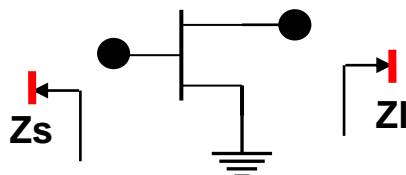
## Elementary Cell Maximum Gain & Stability Characteristics

$T_{ref} = +25^{\circ}\text{C}$ ,  $V_{DS} = +50\text{V}$ ,  $I_{D\_Q} = 80\text{mA}$ , simulated results



## Elementary Cell Load Pull Performances

$T_{ref} = +25^{\circ}\text{C}$ ,  $V_{DS} = +50\text{V}$ ,  $I_{D\_Q} = 80\text{mA}$ , simulated results



The impedances are chosen as a compromise between Output Power, PAE and Stability of the device. Second harmonic of output load and input load has been tuned.

These values are given in the bonding pads reference planes.

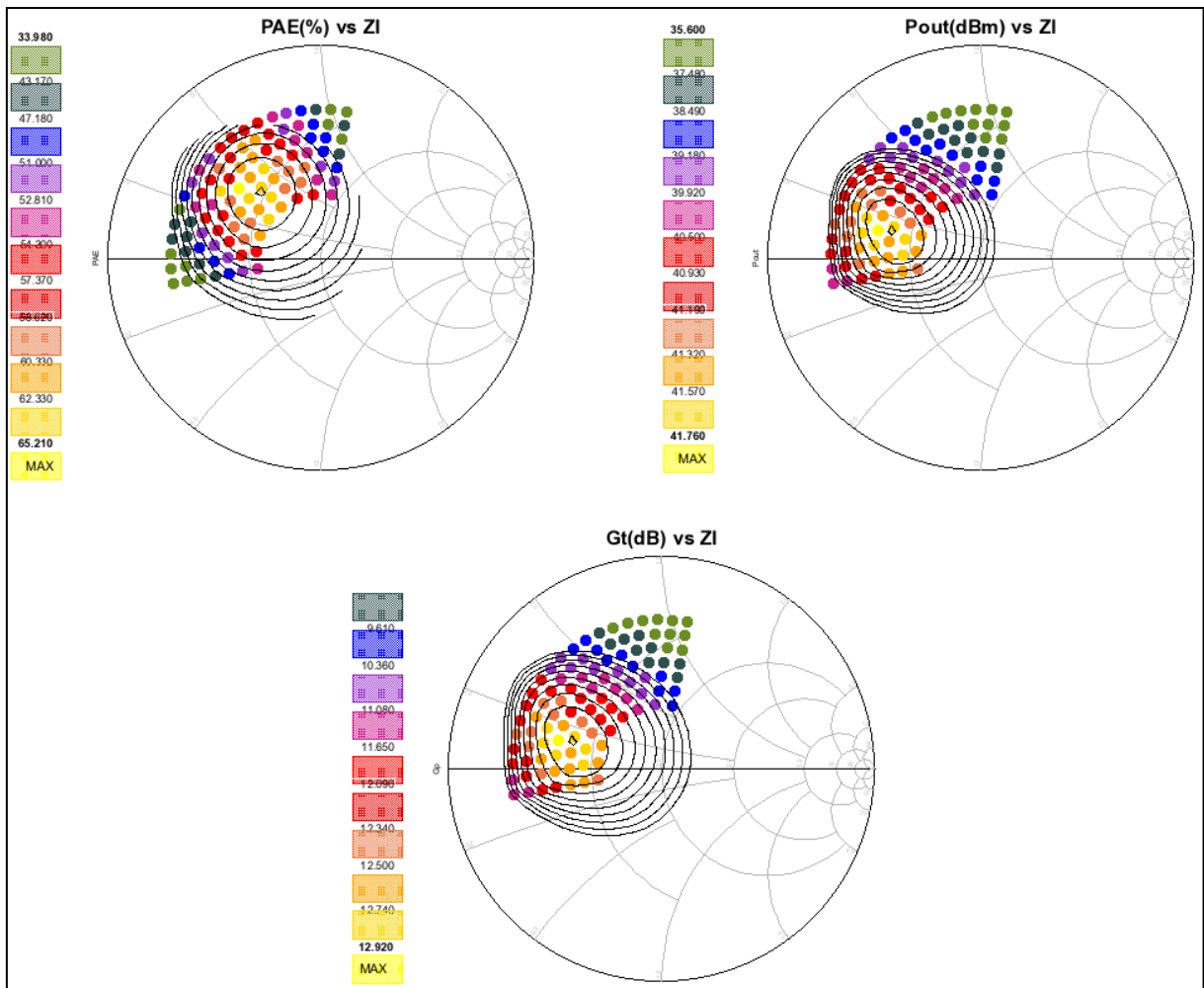
Frequency (GHz)	Zs	Zl	Gain (dB) @PAE <sub>max</sub>	Pout (W) @PAE <sub>max</sub>	PAE <sub>max</sub> (%)
1	17.4 + j7.2	53.7 + j58	17	21	81
2	5.2 + j8.7	19 + j40.6	15	21	79
3	3.36 + j5.95	9.2 + j28.2	14.3	21	76
4	2.9 + j3.14	5.8 + j20.5	12.3	21	70

### Comparison Simulation versus Measurement of Elementary Cell Load Pull Performances

$T_{ref} = +25^{\circ}C$ ,  $V_{GS}$  pulsed mode  $10\mu s - 10\%$ , RF Pulsed width:  $8\mu s$  (inside  $V_{GS}$  pulsed), Freq = 3GHz,  $V_D = 50V$ ,  $I_{D,Q} = 25mA/mm$  (Class AB)

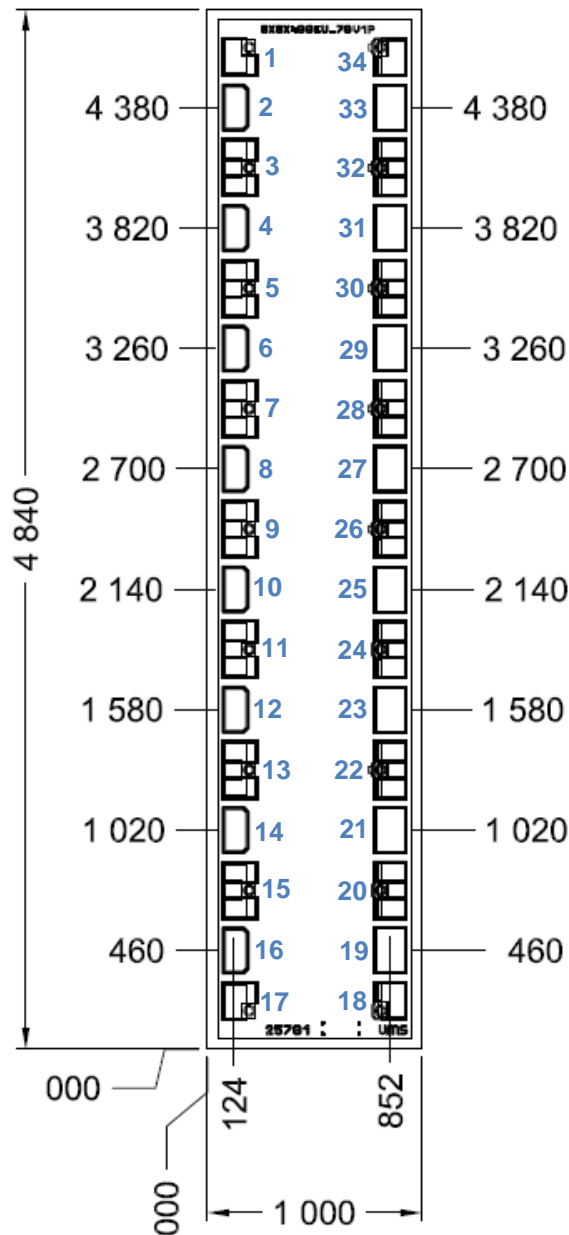
- $Z_{loadH2} = Z_{loadH3} = 50\Omega$
- $Z_{source}$  matched for maximum gain
- On wafer measurement
- Measurement are given in the transistor plan at 5dB of compression
- Simulation in CW conditions

PAE(%), Output Power (dBm) and transducer gain (dB) vs the load impedance



Measurements are represented by multicolour dots and model by black contours.

## Mechanical data



UNITS :  $\mu\text{m}$

Tol :  $\pm 50\mu\text{m}$

Chip thickness:  $100\mu\text{m} \pm 10\mu\text{m}$

GND pads (3, 5, 7, 9, 11, 13, 15, 20, 22, 24, 26, 28, 30, 32) =  $266 \times 150\mu\text{m}^2$

GND pads (1, 17, 18, 34) =  $173 \times 150\mu\text{m}^2$

DC Gate pads (2, 4, 6, 8, 10, 12, 14, 16) =  $212 \times 118\mu\text{m}^2$

DC Drain pads (19, 21, 23, 25, 27, 29, 31, 33) =  $212 \times 118\mu\text{m}^2$



**Notes**



## Qualification domain

This part is qualified according to UMS standards, excluding humid environment.

## User guide for MMIC storage, pick & place, die attach, wire bonding

Refer to the application note AN0001 available at <https://www.ums-rf.com> for general recommendations on chip handling.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

## User guide GaN Power Bars Assembly guide lines

Refer to the application note AN0026 available at <https://www.ums-rf.com> for general recommendations on GaN-on-SiC Transistor handling and assembly.

## Ordering Information

Chip form: CHKA012a99F/00

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