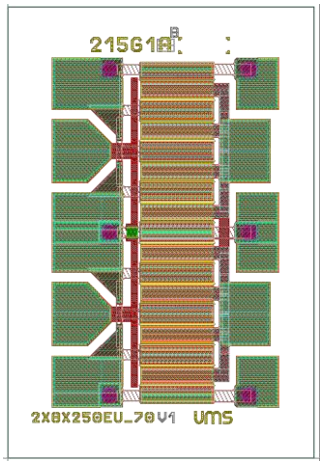
# 20W Power Bar

## GaN HEMT on SiC

## Description

The CHK8101a99F is a 20W Gallium Nitride High Electron Mobility Transistor.

This product offers a general purpose and broadband solution for a variety of RF power applications such as radar and telecommunication.
It is developed on a 0.5µm gate length GaN HEMT technology on SiC substrate and is compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006
It is proposed in a bare die form and requires an external matching circuitry.




## Main Features

- Wide band capability up to 6GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias: $V_{DS}$ up to 50V
- Chip size: 1.05x1.55x0.1mm
- RoHS N°2011/65
- REACh N°1907/2006

## Main Electrical Characteristics

$T_{ref}$ = +25°C, CW mode, Freq = 6GHz, $V_{DS}$ = 50V, $I_{D\_Q}$ = 100mA

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $G_{SS}$ | Small Signal Gain | | 14 | | dB |
| $P_{SAT}$ | Saturated Output Power | | 20 | | W |
| $P_{AE}$ | Max Power Added Efficiency | | 60 | | % |
| $G_{PAE\_MAX}$ | Associated Gain at Max PAE | | 10 | | dB |

These values are deduced from elementary power cell performances.



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## Recommended Operating Ratings (ROR)

$T_{ref}$ = +25°C

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 50 | V | |
| $V_{GS}$ | Gate to Source Voltage | | -1.9 | | V | $V_{DS}$ = 50V, $I_{D\_Q}$ = 100mA |
| $I_{D\_Q}$ | Quiescent Drain Current | | 0.1 | 0.32 | A | $V_{DS}$ = 50V |
| $I_{D\_MAX}$ | Drain Current | | 0.64 | (1) | A | $V_{DS}$ = 50V, compressed mode |
| $I_{G\_MAX}$ | Gate Current in forward mode | | 0 | 16 | mA | DC or Compressed mode |
| $T_{j\_MAX}$ | Junction temperature (1) | | | 200 | °C | |

(1) $T_{ref}$ (back side temperature) and power dissipation must be considered.

## DC Characteristics

Tref= +25°C

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $V_P$ | Pinch-Off Voltage | -2.7 | -2 | -1.5 | V | $V_{DS}$ = 10V, $I_{DS}$ = $I_{DSS}$/100 |
| $I_{D\_SAT}$ | Saturated Drain Current (1) | | 2.4 | | A | $V_{DS}$ = 10V, $V_{GS}$ = 1V |
| $I_{G\_leak}$ | Gate Leakage Current | -0.4 | | | mA | $V_{DS}$ = 50V, $V_{GS}$ = -7V |
| $V_{BDS}$ | Drain-Source Break-down Voltage | | 180 | | V | $V_{GS}$ = -7V, $I_{DS}$ = 20mA |

(1) For information, limited by $I_{D\_MAX}$ and $T_{j\_MAX}$, see on ROR & AMR.

## RF Characteristics

$T_{ref}$ = +25°C, CW mode, Freq = 6GHz, $V_{DS}$ = 50V, $I_{D\_Q}$ = 100mA

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $G_{SS}$ | Small Signal Gain | | 14 | | dB | |
| $P_{SAT}$ | Saturated Output Power | | 20 | | W | |
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## Absolute Maximum Ratings (AMR)

Tref = +25°C [1] [2] [3]

| Symbol | Parameter | Rating | Unit | Note |
|---|---|---|---|---|
| $V_{DS\_Q}$ | Drain-Source Biasing Voltage | 60 | V | |
| $V_{GS\_Q}$ | Gate-Source Biasing Voltage | -10, +2 | V | [4], [5] |
| $I_{G\_MAX}$ | Maximum Gate Current in forward mode | 32 | mA | |
| $I_{G\_MIN}$ | Maximum Gate Current in reverse mode | -2 | mA | |
| $I_{D\_MAX}$ | Maximum Drain Current | See note | | [4] |
| $P_{IN}$ | Maximum Input Power | See note | | [5] |
| $T_{jmax}$ | Maximum Junction Temperature | 230 | °C | |
| $T_{STG}$ | Storage Temperature | -55 to +150 | °C | |
| $T_{ref}$ | Back Side Operating Temperature | See note | °C | [4] |

[1] Operation of this device above anyone of these parameters may cause permanent damage.

[2] Duration < 1s.

[3] The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

[4] Max junction temperature must be considered.

[5] Linked to and limited by $I_{G\_MAX}$ & $I_{G\_MIN}$ values. Maximum input power depends on frequency and should not exceed 2dB above PAE_max.

## Biasing procedure

1. Bias power bar gate voltage at $V_{GS}$ close to $V_p$ (Typically: $V_{GS} \approx -5V$)
2. Apply $V_{DS}$ bias voltage (Typically: $V_{DS} = 50V$)
3. Increase $V_{GS}$ up to quiescent bias drain current $I_{D\_Q}$

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.
A drain current control is recommended on the biasing network.



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## Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (Tj). This temperature is defined as the peak temperature in the channel area.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHK8101a99F is fabricated (GaN Power HEMT 0.5µm).
The temperature Tb is defined as the chip back side temperature
The thermal resistance (Rth) is given for the full power bar, in “equivalent” CW operating mode and in two different configurations as given in the table. The device assembly must be adapted to the operating mode. Thermal analysis is recommended. More information is available on request.

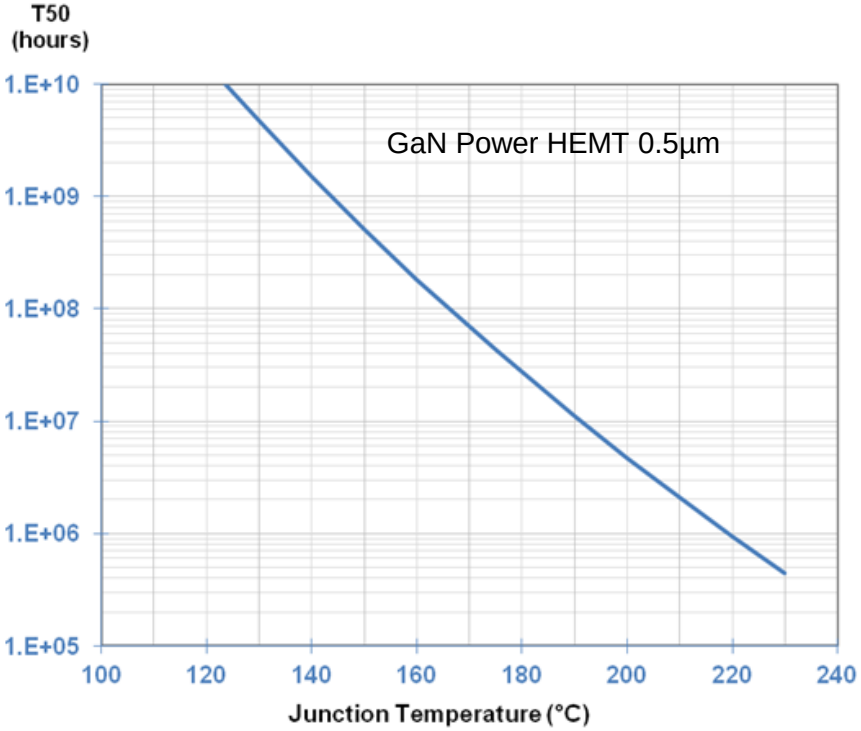
| Parameters | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Typical Thermal Resistance | Rth | Bare die characteristic<br>Tb = 100°C<br>Pdiss = 16W<br>CW | 3.3 | °C/W |
| Junction Temperature | Tj | | 153 | °C |

The back side temperature (Tb) is considered uniform on all the surface

| | | | | |
|---|---|---|---|---|
| Typical Thermal Resistance | Rth | Bare die on carrier characteristic<br>Tc = 85°C<br>Pdiss = 16W<br>CW | 5.9 | °C/W |
| Junction Temperature | Tj | | 180 | °C |

The reference temperature (Tc) is defined on the carrier back side. The power bar is mounted on carrier plate (20µm Au/Sn soldering + 1.5mm Cu/Mo/Cu).

**Median Life Time versus Junction Temperature**



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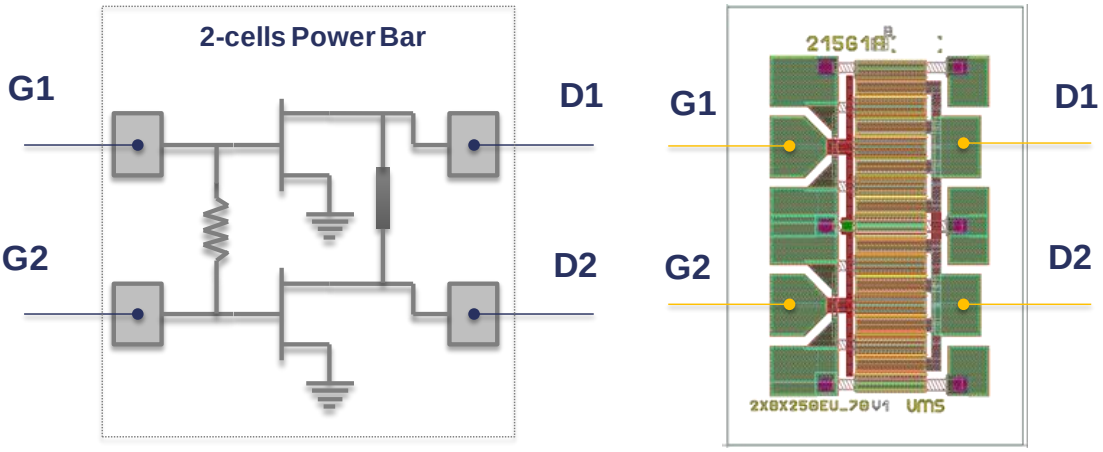
## Power Bar Description

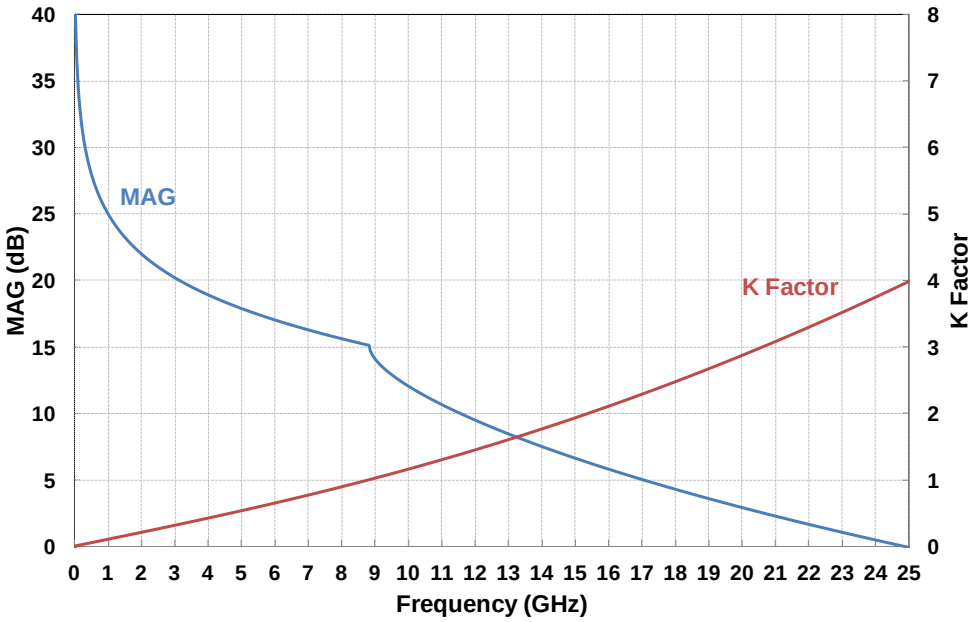
The CHK8101a99F is composed of 2 elementary 10W cells. These cells are connected together with a specific network providing a good compromise between performances and stability (resistance between gates and short circuit on drains). The reference planes are on the center of the bonding pads.

A multiport non-linear model is available on request.




## Elementary Cell Maximum Gain & Stability Characteristics

$T_{ref}$ = +25°C, $V_{DS}$ = +50V, $I_{D\_Q}$ = 50mA, simulated results



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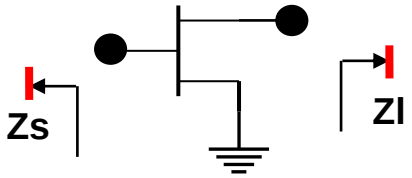
## Elementary Cell Load Pull Performances

$T_{ref}$ = +25°C, $V_{DS}$ = +50V, $I_{D\_Q}$ = 50mA, simulated results




The impedances are chosen as a compromise between Output Power, PAE and Stability of the device. Second harmonic of output load and input load has been tuned.
These values are given in the bonding pads reference plane.

| Frequency (GHz) | Zs | Zl | Gain (dB) @$PAE_{max}$ | $PAE_{max}$ (%) | Pout (W) @$PAE_{max}$ |
|---|---|---|---|---|---|
| 1 | 7.9+ j28.4 | 48+ j60 | 20.4 | 79 | 13.8 |
| 2 | 3.7+ j14.2 | 32.8+ j65.1 | 19.6 | 79 | 14.5 |
| 3 | 2.3+ j8.6 | 15.1+ j44.6 | 17.7 | 77 | 14.5 |
| 4 | 1.87+ j5.5 | 9.4+ j30 | 16.4 | 71 | 13.7 |
| 5 | 1.5+ j3.9 | 6+ j23.5 | 15.2 | 65.5 | 13.3 |
| 6 | 1.49+ j2.3 | 4.37+ j18.6 | 13.2 | 60.4 | 13.3 |



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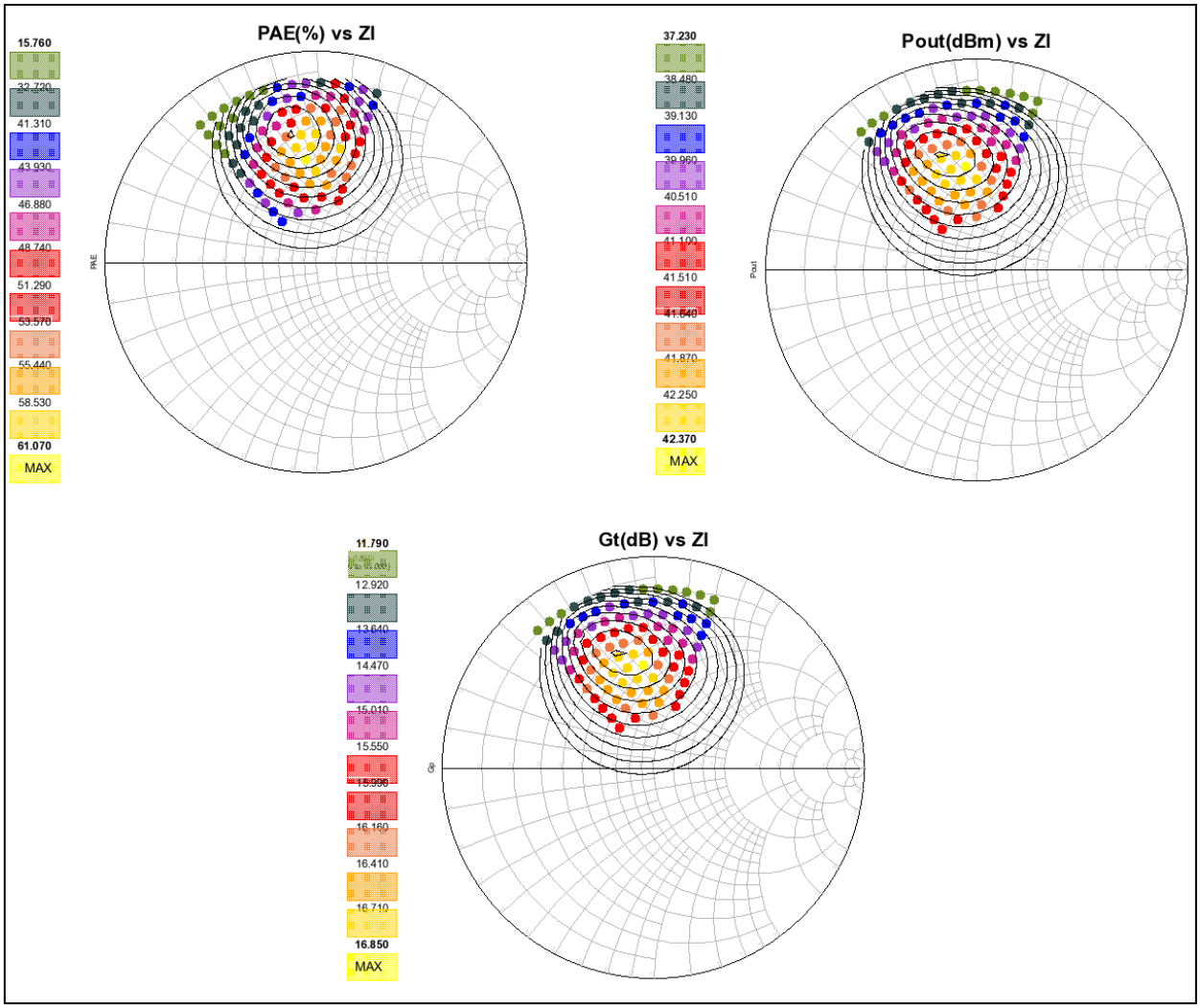
## Comparison Simulation versus Measurement of Elementary Cell Load Pull Performances

$T_{ref}$ = +25°C, $V_{GS}$ pulsed mode 10µs - 10%, RF Pulsed width: 8µs (inside $V_{GS}$ pulsed), Freq = 3GHz, $V_{DS}$ = 50V, $I_{D\_Q}$ = 25mA/mm (Class AB)

- ZloadH2 = ZloadH3 = 50Ω
- Zsource matched for maximum gain
- On wafer measurement
- Measurement are given in the transistor plan at 5dB of compression
- Simulation in CW conditions

**PAE(%), Output Power (dBm) and transducer gain (dB) vs the load impedance**




Measurements are represented by multicolour dots and model by black contours.



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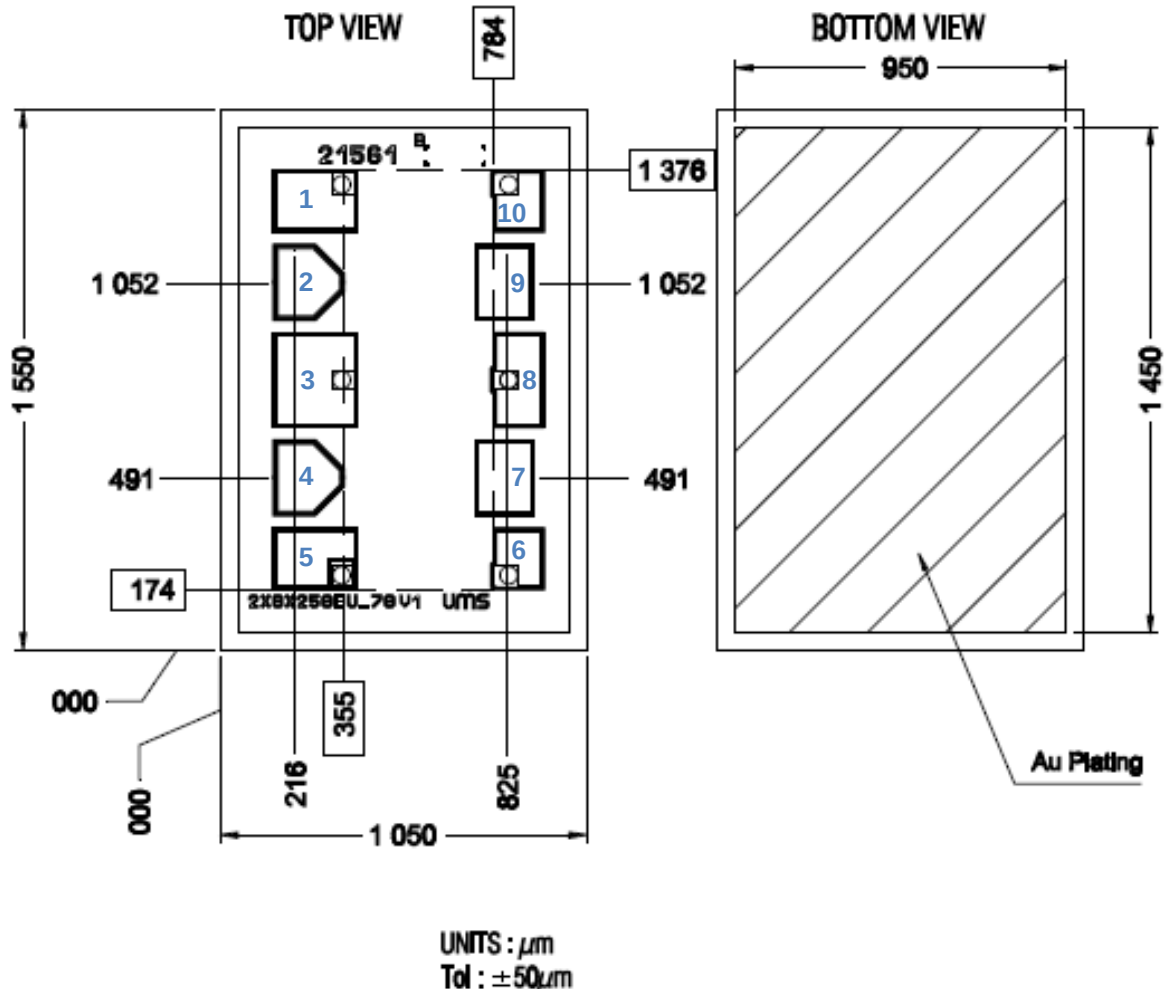
## Mechanical data




Chip thickness: 100µm +/- 10 µm

GND pads (3, 8) = 266x236µm²
GND pads (1, 5) = 171x236µm²
GND pads (6, 10) = 171x139µm²
DC Gate pads (2, 4) = 212 x 150µm²
DC Drain pads (7, 9) = 212 x 150µm²



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## Notes



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## Qualification domain

This part is qualified according to UMS standards, excluding humid environment.

## User guide for MMIC storage, pick & place, die attach, wire bonding

Refer to the application note AN0001 available at https://www.ums-rf.com for general recommendations on chip handling.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

## Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

## User guide GaN Power Bars Assembly guide lines

Refer to the application note AN0026 available at https://www.ums-rf.com for general recommendations on GaN-on-SiC Transistor handling and assembly.

## Ordering Information

| | |
|---|---|
| Chip form: | CHK8101a99F/00 |





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