

## 15W Power Packaged Transistor

### GaN HEMT on SiC in SMD leadless package

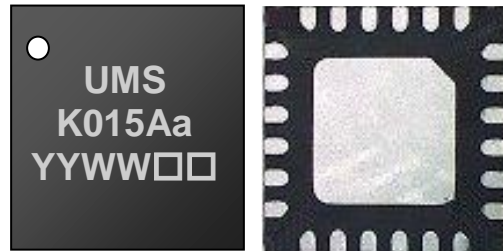
#### Description

The CHK015AaQIA is an unmatched packaged Gallium Nitride High Electron Mobility Transistor.

It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication.

The CHK015AaQIA is developed on a 0.5 $\mu$ m gate length GaN HEMT process. It requires an external matching circuitry.

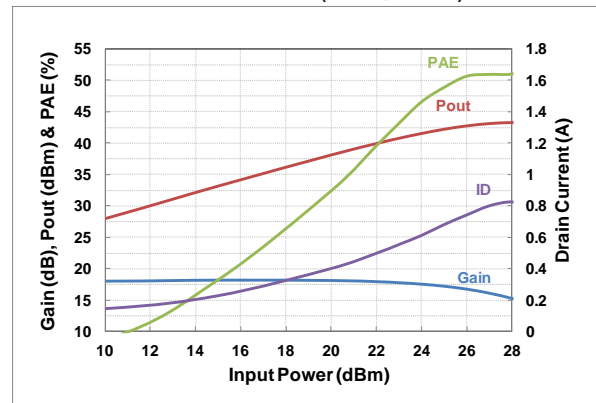
It is proposed in low cost plastic package providing low parasitic and low thermal resistance.



#### Main Features

- Wide band capability: up to 4GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias:  $V_{DS}$  up to 50V
- Low cost package: 14L-DFN3x4
- MTTF > 10<sup>6</sup> hours @  $T_j = 200^\circ\text{C}$
- RoHS N°2011/65
- REACH N°1907/2006

$V_{DS} = 50\text{V}$ ,  $I_{D,Q} = 75\text{mA}$ , Freq = 2.9GHz  
Pulsed mode (1ms, 10%)



#### Main Electrical Characteristics<sup>(1)</sup>

$T_{amb.} = +25^\circ\text{C}$ , Pulsed mode, F = 2.9GHz,  $V_{DS} = 50\text{V}$ ,  $I_{D,Q} = 75\text{mA}$

Symbol	Parameter	Min	Typ	Max	Unit
$G_{SS}$	Small Signal Gain	16	18		dB
$P_{SAT}$	Saturated Output Power	15	20		W
PAE	Max Power Added Efficiency		55		%
$I_{D,SAT}$	Saturated Drain Current		800		mA

<sup>(1)</sup>: These values are the intrinsic performance of the packaged device.

## Recommended DC Operating Ratings

T<sub>case</sub>= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V <sub>DS</sub>	Drain to Source Voltage			50	V	
V <sub>GS_Q</sub>	Gate to Source Voltage		-1.9		V	V <sub>D</sub> =50V. I <sub>D_Q</sub> =75mA
I <sub>D_Q</sub>	Quiescent Drain Current		75	320	mA	V <sub>D</sub> =50V
I <sub>D_MAX</sub>	Drain Current		800	(1)	mA	V <sub>D</sub> =50V. compressed mode
I <sub>G_MAX</sub>	Gate Current (forward mode)		0	16	mA	DC or Compressed mode
T <sub>op</sub>	Operating temperature range	-40		+85	°C	
T <sub>j_MAX</sub>	Junction temperature <sup>(1)</sup>			200	°C	

(1) Power dissipation must be considered

## DC Characteristics

T<sub>case</sub>= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V <sub>P</sub>	Pinch-Off Voltage	-2.7	-2	-1.5	V	V <sub>D</sub> =10V. I <sub>D</sub> = I <sub>DSS</sub> /100
I <sub>D_SAT</sub>	Saturated Drain Current		2.4 (1)		A	V <sub>D</sub> =10V. V <sub>G</sub> =1V
I <sub>G_leak</sub>	Gate Leakage Current (reverse mode)	-0.8			mA	V <sub>D</sub> =50V. V <sub>G</sub> =-7V
V <sub>BDS</sub>	Drain-Source Break-down Voltage		180		V	V <sub>G</sub> =-7V. I <sub>D</sub> =20mA

(1) For information, limited by I<sub>D\_MAX</sub>. see on Absolute Maximum Ratings

## RF Characteristics

T<sub>case</sub>= +25°C. Pulsed mode

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G <sub>SS</sub>	Small Signal Gain @ 2.9GHz	16	18		dB	V <sub>D</sub> =50V. I <sub>D_Q</sub> =75mA
P <sub>SAT</sub>	Saturated Output Power	15	20		W	V <sub>D</sub> =50V. I <sub>D_Q</sub> =75mA
PAE	Max PAE @ 2.9GHz		55		%	V <sub>D</sub> =50V. I <sub>D_Q</sub> =75mA
G <sub>PAE_MAX</sub>	Associated Gain at Max PAE @ 2.9GHz		15		dB	V <sub>D</sub> =50V. I <sub>D_Q</sub> =75mA

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB.

The typical performance achievable in more than 10% frequency band around 3GHz was demonstrated using the reference board 61502522 presented hereafter.

## Absolute Maximum Ratings

T<sub>case</sub> = +25°C<sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

Symbol	Parameter	Rating	Unit	Note
V <sub>DS</sub>	Drain-Source Biasing Voltage	60	V	
V <sub>GS_Q</sub>	Gate-Source Biasing Voltage	-10. +2	V	
I <sub>G_MAX</sub>	Maximum Gate Current in forward mode	32	mA	
I <sub>G_MIN</sub>	Maximum Gate Current in reverse mode	-2	mA	
I <sub>D_MAX</sub>	Maximum Drain Current	3	A	(4)
P <sub>IN</sub>	Maximum Input Power	30	dBm	(5)
T <sub>j</sub>	Junction Temperature	230	°C	
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C	
T <sub>Case</sub>	Case Operating Temperature	-40 to +100	°C	(4)

<sup>(1)</sup> Operation of this device above any one of these parameters may cause permanent damage.

<sup>(2)</sup> Duration < 1s.

<sup>(3)</sup> The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other. Otherwise deterioration or destruction of the device may take place.

<sup>(4)</sup> Max junction temperature must be considered

<sup>(5)</sup> Linked to and limited by I<sub>G\_MAX</sub> & I<sub>G\_MIN</sub> values. Maximum input power depends on frequency and should not exceed 2dB above PAE<sub>max</sub>.

## Biasing procedure

1. Bias power bar gate voltage at V<sub>GS</sub> close to V<sub>p</sub> (Typically: V<sub>GS</sub> ≈ -5V)
2. Apply V<sub>DS</sub> bias voltage (Typically: V<sub>DS</sub> = 50V)
3. Increase V<sub>GS</sub> up to quiescent bias drain current I<sub>D\_Q</sub>

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.

A drain current control is recommended on the biasing network.

## Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature ( $T_j$ ). This temperature is defined as the peak temperature in the channel area. This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime (see graph below) and activation energy for the particular technology on which the CHK015AaQIA is fabricated (GaN Power HEMT 0.5 $\mu$ m).

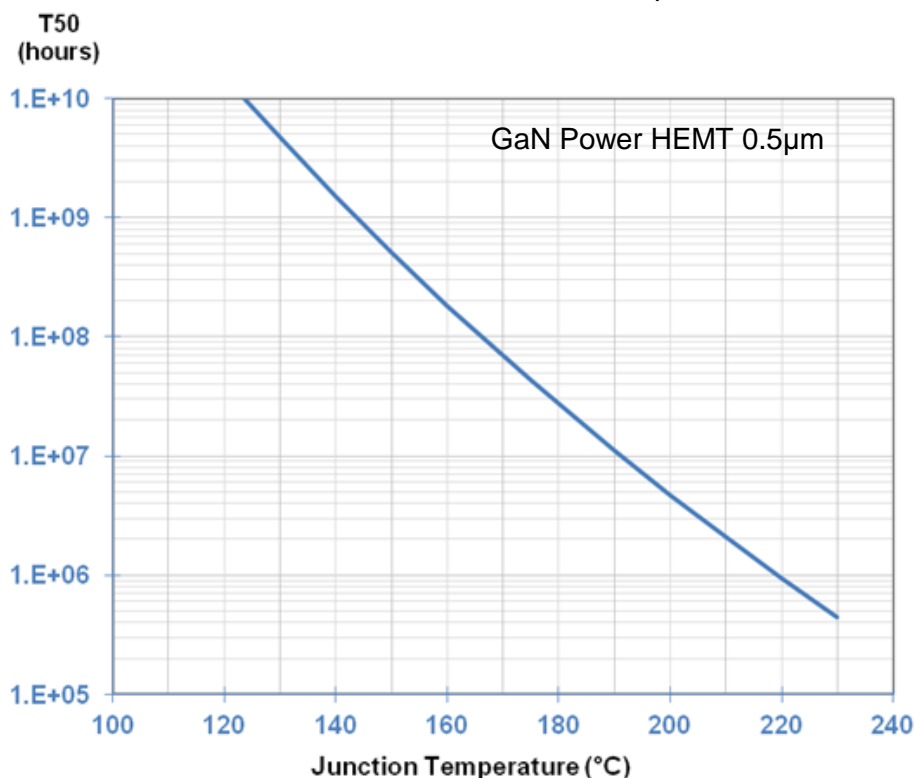
The temperature  $T_{case}$  is defined as the package back side temperature.

The thermal resistance ( $R_{th}$ ) is given in “equivalent” CW operating mode between junction and  $T_{case}$ .

Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	$R_{th}$	Packaged Device characteristic $T_{case} = 85^{\circ}\text{C}$	5	$^{\circ}\text{C}/\text{W}$
Junction Temperature	$T_j$	$P_{diss} = 20\text{W}$ CW	185	$^{\circ}\text{C}$

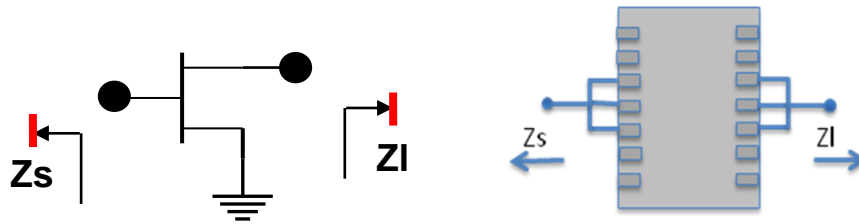
The package back side temperature is considered uniform.

Median Life Time versus Junction Temperature



### Simulated Source and Load Impedances

$V_{DS} = 50V$ ,  $I_{D_Q} = 75mA$



Frequency (MHz)	Zs	Zl	Pout (W)	PAE (%)
1000	$2.4 + j12.3$	$30 + j25$	22	66
2000	$1.5 + j3.5$	$14.7 + j19.7$	21	64
3000	$1.5 - j0.8$	$11 + j12.8$	20.5	60
4000	$1.2 - j4.3$	$6.2 + j8.3$	20	59

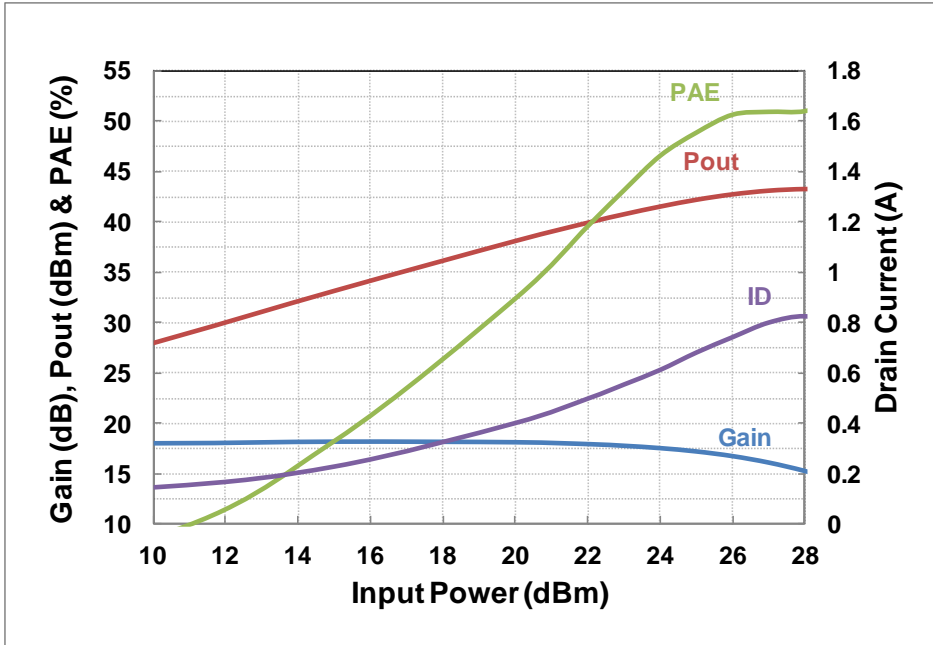
The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device. These values are given in the reference plane defined by the connection between the transistor leads and the PCB according to the footprint above mentioned.

## Typical Measured Performance on Evaluation Board (ref 61502522)

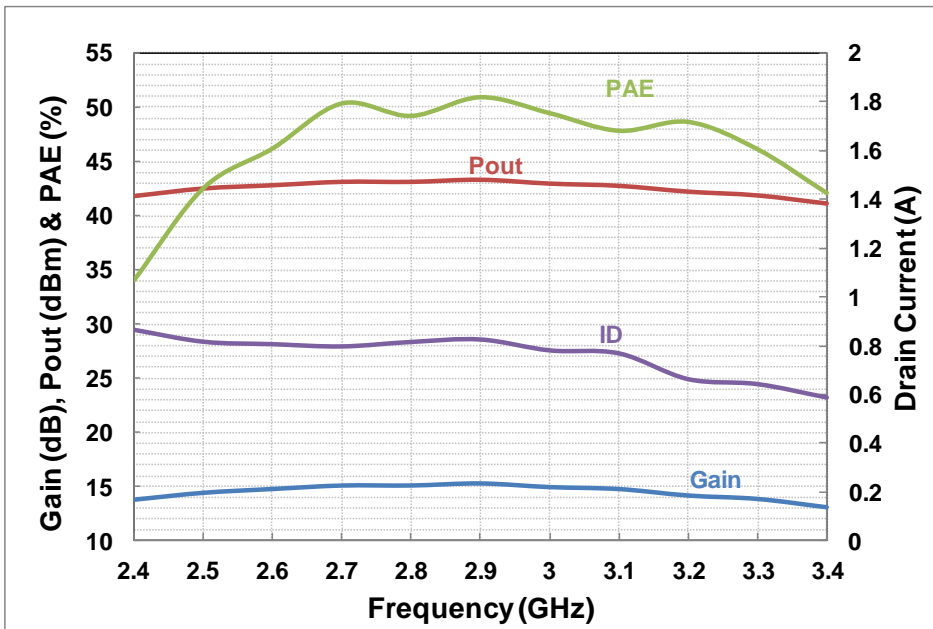
Calibration and measurements are done on the connector access planes of the evaluation boards.

Tamb. = +25°C, Pulsed Mode <sup>(1)</sup>, V<sub>DS</sub> = 50V, I<sub>D\_Q</sub> = 75mA

**Pout. PAE. Gain & ID @ Freq = 2.9GHz**



**Pout. PAE. Gain & ID @ Pin = 28dBm**



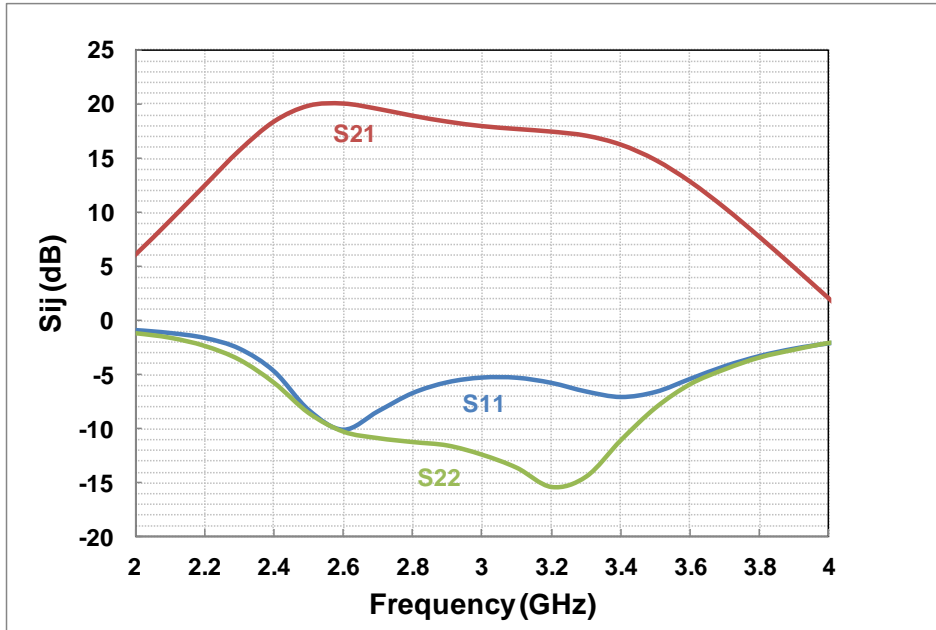
<sup>(1)</sup> Input RF and gate voltage are pulsed. Conditions are 1ms width. 10% duty cycle and 1µs offset between DC and RF pulse.

**Typical Measured Performance on Evaluation Board (ref 61502522)**

Calibration and measurements are done on the connector access planes of the evaluation boards.

Tamb. = +25°C, CW mode,  $V_{DS} = 50V$ ,  $I_{D_Q} = 75mA$

**S parameters versus frequency**

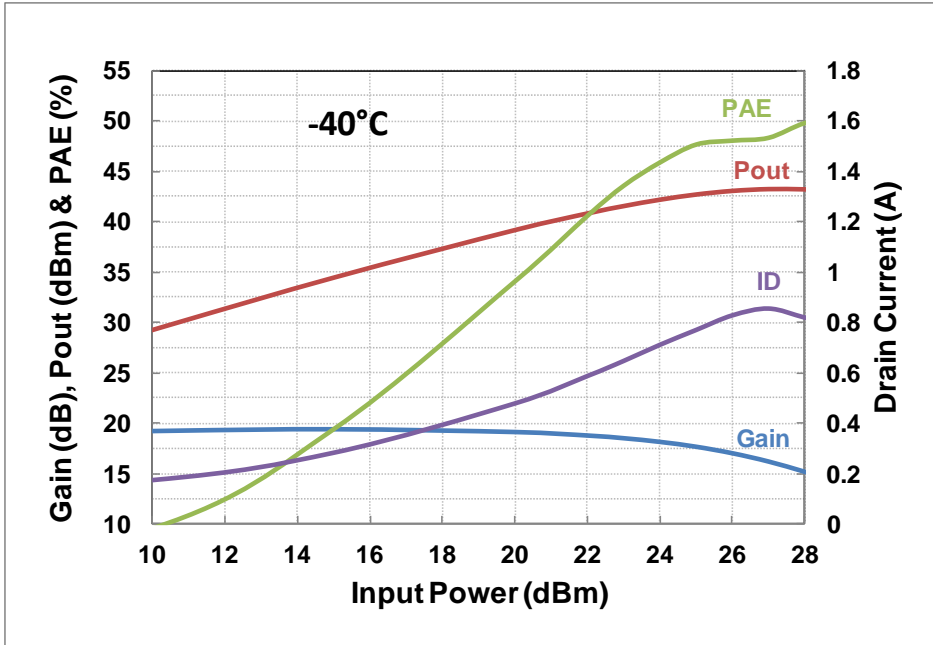


## Typical Measured Performance in Temperature (Evaluation Board)

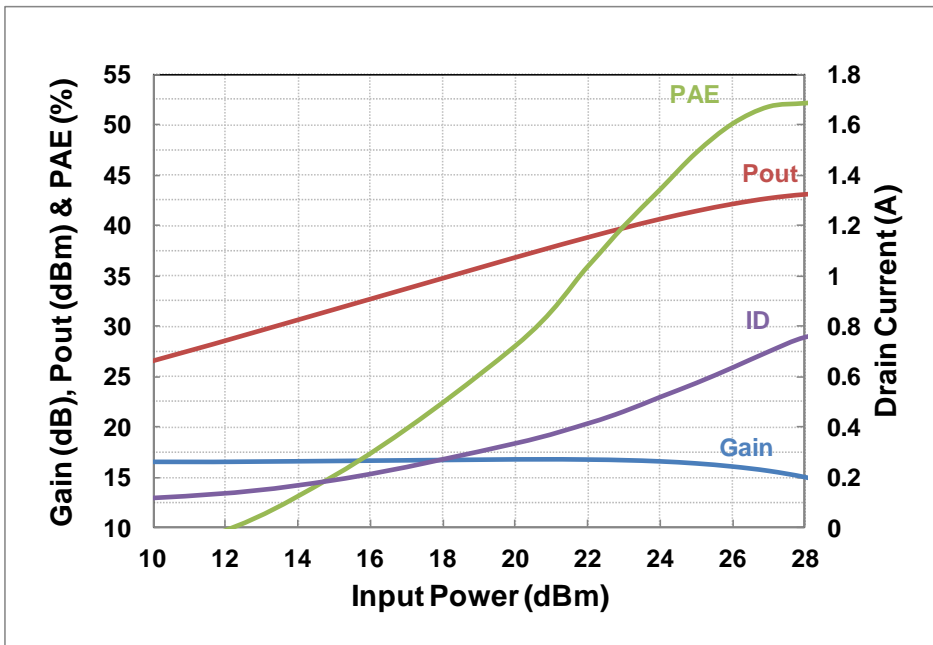
Calibration and measurements are done on the connector access planes of the evaluation boards.

Tamb. = -40°C & +85°C, Pulsed Mode <sup>(1)</sup>, V<sub>DS</sub> = 50V, I<sub>D\_Q</sub> = 75mA

**Pout, PAE, Gain & Id @ 2.9GHz & -40°C**



**Pout, PAE, Gain & Id @ 2.9GHz & +85°C**



<sup>(1)</sup> Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1µs offset between DC and RF pulse.

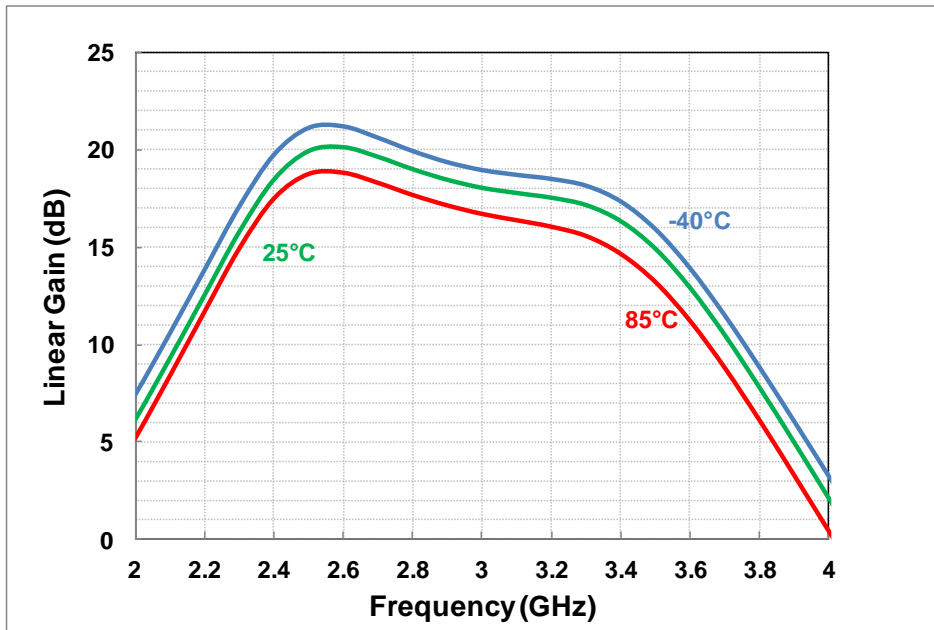


**Typical Measured Performance in Temperature (Evaluation Board)**

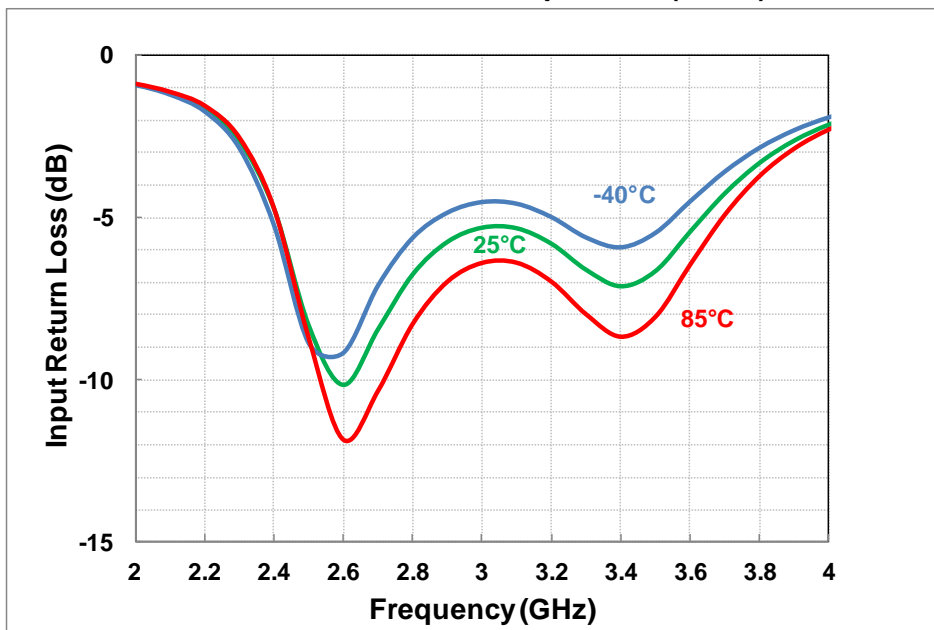
Calibration and measurements are done on the connector access planes of the evaluation boards.

Tamb. = -40°C, +25°C, +85°C, CW mode, V<sub>DS</sub> = 50V, I<sub>D\_Q</sub> = 75mA (fixed @ +25°C)

**Linear Gain versus temperature  
with I<sub>D\_Q</sub> fixed @ each temperature (75mA)**



**Input Return Loss versus temperature  
with I<sub>D\_Q</sub> fixed @ each temperature (75mA)**

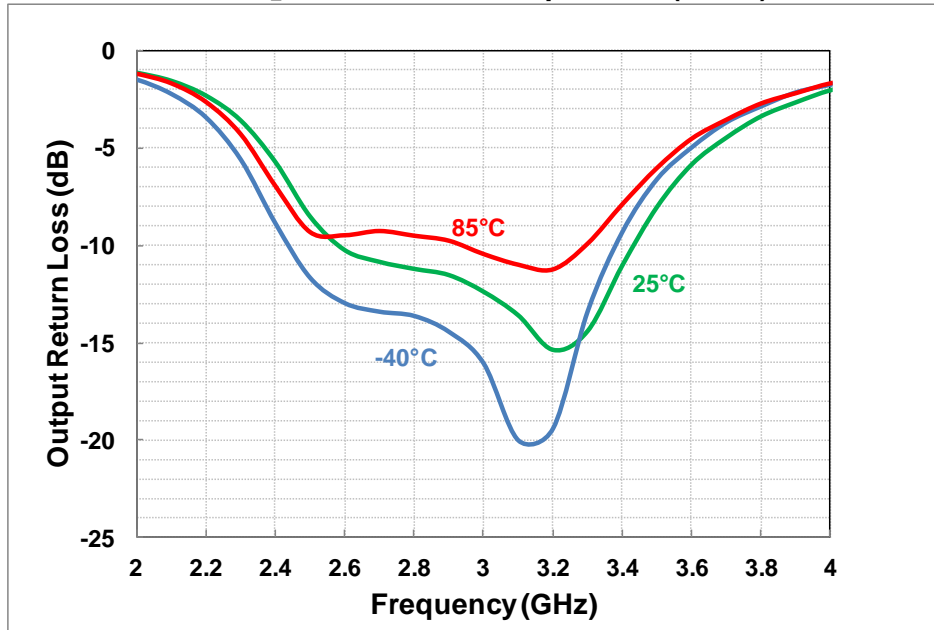


## Typical Measured Performance in Temperature (Evaluation Board)

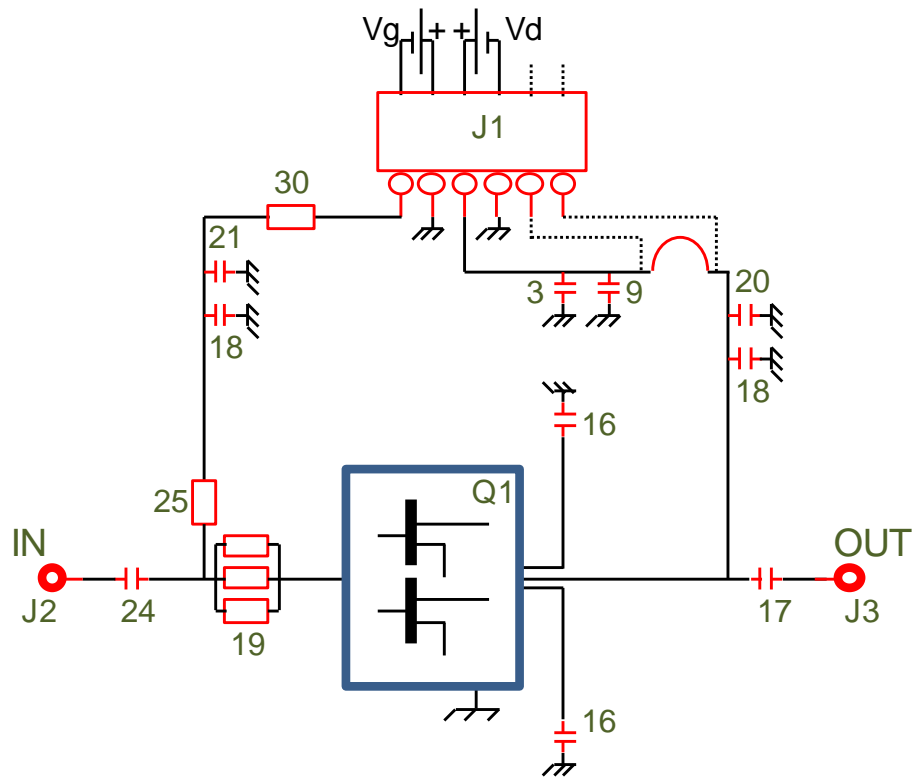
Calibration and measurements are done on the connector access planes of the evaluation boards.

Tamb. = -40°C, +25°C, +85°C, CW mode.  $V_{DS} = 50V$ ,  $I_{D,Q} = 75mA$  (fixed @ +25°C)

**Output Return Loss versus temperature  
with  $I_{D,Q}$  fixed @ each temperature (75mA)**



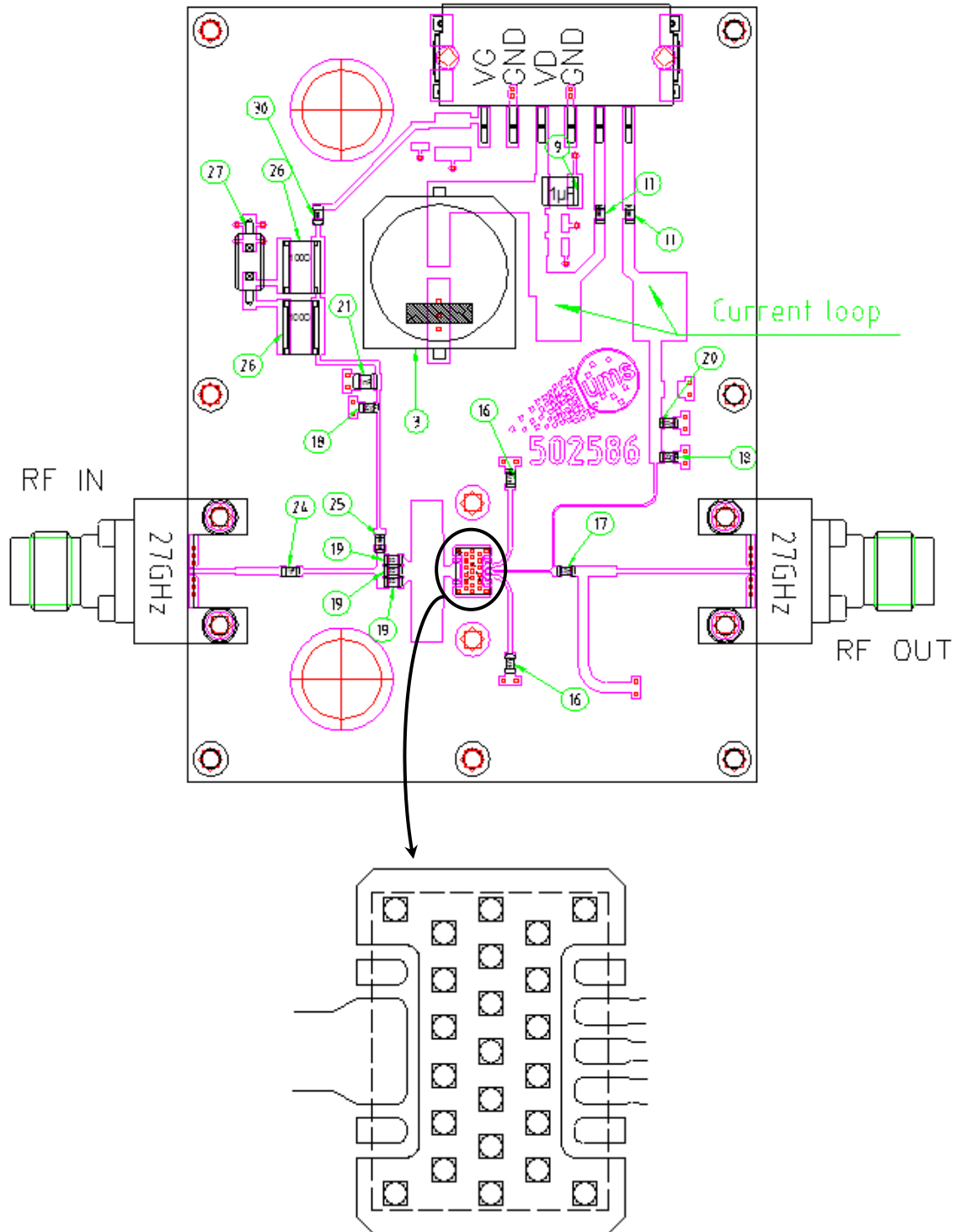
## Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61502522)



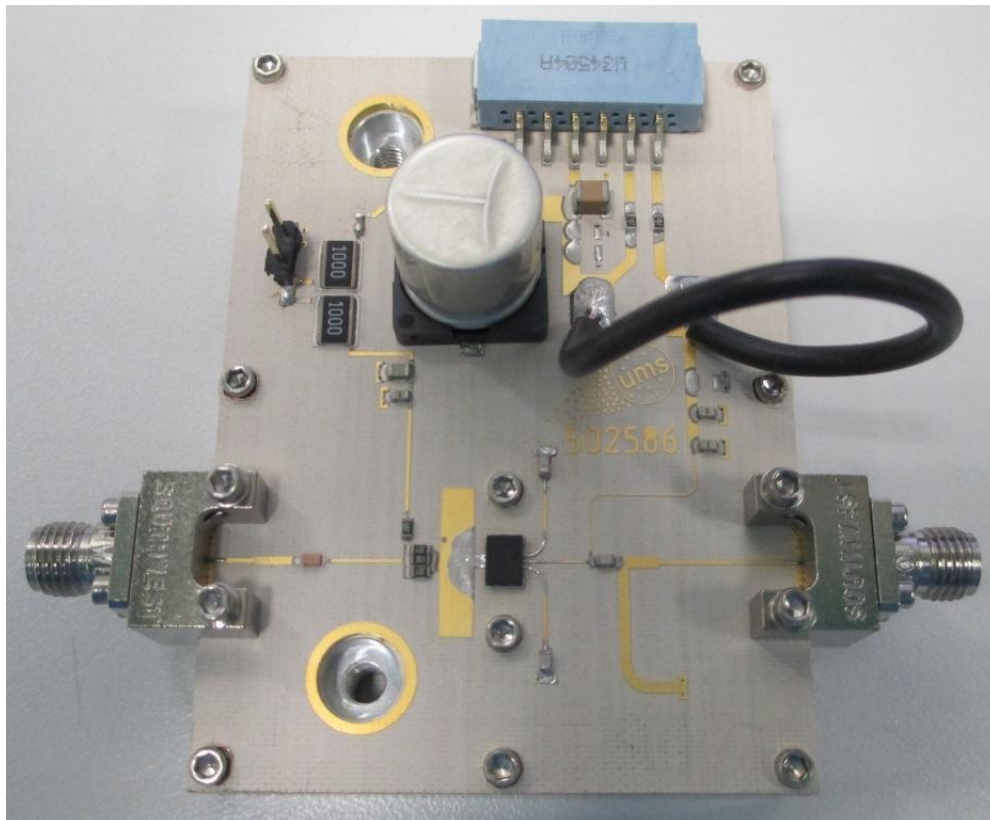
## Demonstration Amplifier Bill of Materials (Ref. 61502522)

Designator	Type	Value - Description	Qty
24	Capacitor	1pF. +/- 0.1pF. 0603	1
16	Capacitor	4.7pF. +/- 0.25pF. 0603	1
17	Capacitor	3.9pF. +/- 0.25pF. 0603	1
18	Capacitor	20pF. +/- 5%. 0603	2
20	Capacitor	100pF. +/- 5%. 0603	1
21	Capacitor	1nF. +/- 5%. 0805	1
9	Capacitor	1μF. +/- 10%. 1210	1
3	Capacitor	68μF. +/- 20%	1
25	Resistor	49.9Ω. +/- 1%. 0603	1
19	Resistor	3Ω +/- 1%. 0603	3
30	Resistor	100Ω +/- 1%. 0603	1
J1	Connector	CMS 6cts	1
J2. J3	Connector	SMA	2
Q1	Packaged Transistor	CHK015A-QIA	1
-	PCB	TACONIC RF35P h=0.203mm	-

## Demonstration Amplifier Circuit Outline (Ref. 61502522)



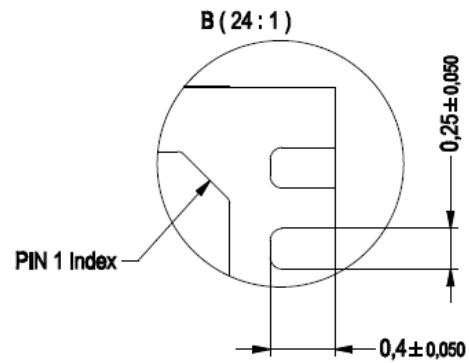
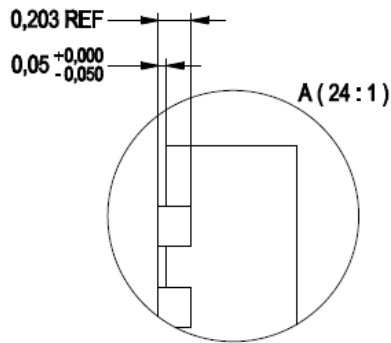
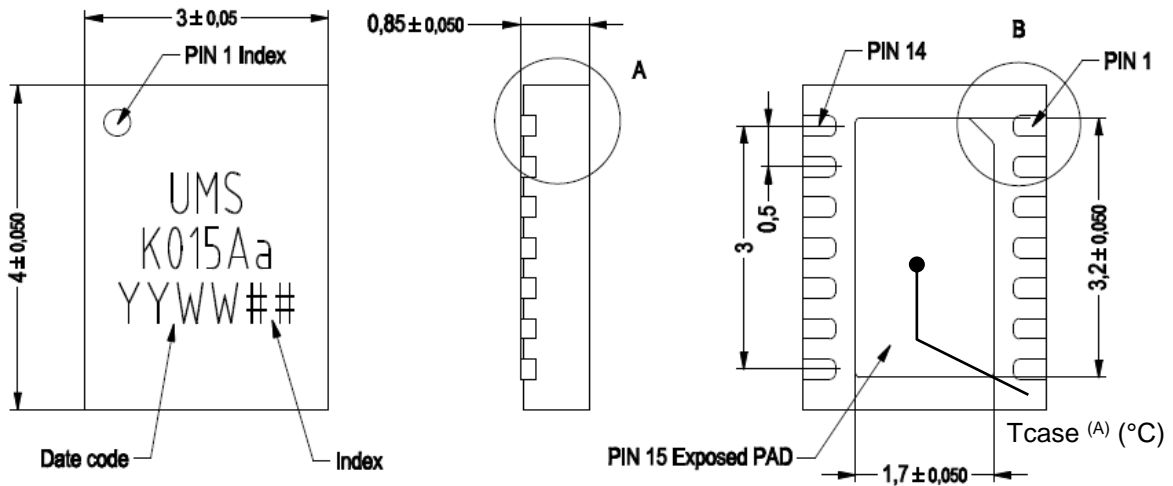
**Demonstration Amplifier Circuit (Ref. 61502522)**



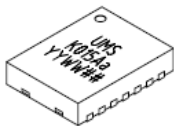
# CHK015AaQIA

# 15W Power Packaged Transistor

## Package outline



Unit : mm  
 Finish : Ni-Pd-Au  
 Lead free ( Green)



1- Nc	6- Nc	11- D2
2- Nc	7- Nc	12- D1
3- G1	8- GND	13- Nc
4- G2	9- Nc	14- GND
5- G3	10- D3	15- GND

**Notes**



## Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

DFN 3x4 package:

CHK015AaQIA/XY

Stick: XY = 20

Tape & reel: XY = 21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**