10-27GHz Bidirectionnal Detector

GaAs Monolithic Microwave IC

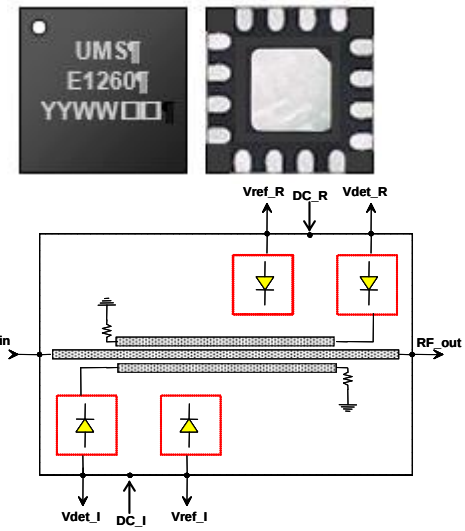
Description

The CHE1260-QAG is a bidirectionnal detector that integrates a passive bidirectionnal coupler, two matched detector diodes and two reference diodes.

It allows the measurement of transmitted and reflected power. It is designed for a wide range of applications where an accurate transmitted power control is required, typically commercial communication systems.

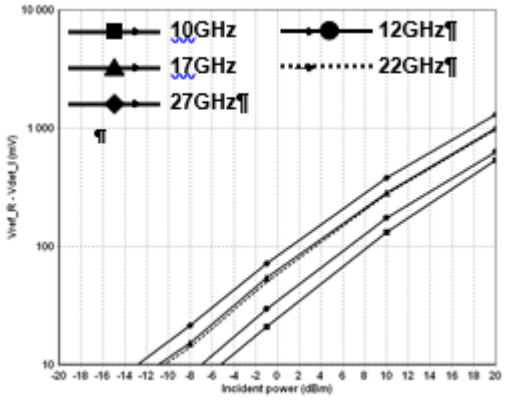
The circuit is manufactured with a Schottky diode MMIC process, 1µm gate length, via holes through the substrate and air bridges.

It is supplied in leadless SMD package.



Main Features

- Wide frequency range 10-27GHz
- Bidirectionnal detection
- 30dB dynamic range
- ESD protected
- 16L-QFN3x3 SMD package
- MSL1



Main Electrical Characteristics

Tamb = +25°C, VDC = +4.5V (on DC_I and DC_R)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	10		27	GHz
IL	Insertion Loss		1		dB
Dr	Dynamic Range		15		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics

Tamb = +25°C, VDC = +4.5V (on DC_I and DC_R)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	10		27	GHz
IL	Insertion Loss		1		dB
Cd	Coupler Directivity		15		dB
Dr	Dynamic Range : 10 - 12GHz 12 - 24GHz 24 - 27GHz		 15 18 15		 dB dB dB
Pd	Power detection : 10 - 17GHz 17 - 21GHz 21 - 24GHz 24 - 27GHz	 -1 -3 -6 -8			 dBm dBm dBm dBm
Vdetect_I	Voltage detection from transmitted power Vref_R – Vdet_I From Pd_min to Pd_max	20		3500	mV
Vdetect_R	Voltage detection from reflected power Vref_I – Vdet_R From Pd_min to Pd_max	20		3500	mV
RLin	Input return loss		-12	-9	dB
RLout	Output return loss		-12	-9	dB
VDC	Bias Voltage		4.5		V
IDC	Bias Current (on ports DC_I or DC_R)	25	33	45	µA

These values are representative of on board measurements as defined in notes, with 100kΩ resistor in parallel on pads Vdet_I, Vref_I, Vdet_R and Vref_R (see notes).

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
VDC	Bias voltage (on ports DC_I and DC_R)	6	V
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C
P_max	Maximum power (for transmitted and/or reflected power)	30	dBm

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

Thermal datas: Pdc_max = 50µA x 1V = 50µW and PRF_max = 20mW
Tj_max = 175°C for maximum ratings

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Typical Package Sij parameters

Tamb = +25°C, Vdc = +4.5V (on DC_I and DC_R), 100kΩ resistor in parallel on pads Vdet_I, Vref_I, Vdet_R and Vref_R (see notes).

Freq (GHz)	dB(S11)	Ph(S11) (°)	dB(S12)	Ph(S12) (°)	dB(S21)	Ph(S21) (°)	dB(S22)	Ph(S22) (°)
2	-27.2	43	-0.2	-35	-0.2	-35	-26.8	34
3	-24.0	33	-0.2	-53	-0.2	-53	-23.8	21
4	-21.7	18	-0.3	-70	-0.3	-70	-21.3	5
5	-19.9	3	-0.3	-87	-0.3	-88	-19.6	-11
6	-18.4	-15	-0.4	-105	-0.4	-105	-18.2	-27
7	-17.3	-33	-0.4	-122	-0.4	-122	-16.9	-43
8	-16.1	-51	-0.5	-140	-0.5	-140	-15.8	-58
9	-15.2	-70	-0.5	-157	-0.5	-157	-14.9	-74
10	**-14.5**	**-88**	**-0.6**	**-174**	**-0.6**	**-174**	**-14.1**	**-90**
11	**-13.7**	**-107**	**-0.7**	**168**	**-0.7**	**168**	**-13.3**	**-105**
12	**-13.0**	**-124**	**-0.7**	**151**	**-0.7**	**151**	**-12.7**	**-121**
13	**-12.5**	**-141**	**-0.8**	**134**	**-0.8**	**134**	**-12.3**	**-138**
14	**-12.3**	**-157**	**-0.8**	**117**	**-0.8**	**117**	**-12.3**	**-155**
15	**-12.6**	**-172**	**-0.8**	**100**	**-0.8**	**100**	**-12.7**	**-172**
16	**-13.3**	**172**	**-0.8**	**82**	**-0.8**	**82**	**-13.6**	**170**
17	**-14.6**	**157**	**-0.7**	**65**	**-0.7**	**65**	**-15.2**	**150**
18	**-17.5**	**142**	**-0.7**	**47**	**-0.7**	**47**	**-18.2**	**127**
19	**-22.5**	**131**	**-0.7**	**29**	**-0.7**	**29**	**-23.6**	**100**
20	**-34.9**	**161**	**-0.7**	**11**	**-0.7**	**11**	**-31.9**	**23**
21	**-24.9**	**-105**	**-0.7**	**-8**	**-0.7**	**-8**	**-25.1**	**-73**
22	**-18.8**	**-116**	**-0.8**	**-26**	**-0.8**	**-26**	**-19.6**	**-105**
23	**-15.9**	**-132**	**-0.9**	**-45**	**-0.9**	**-45**	**-17.3**	**-131**
24	**-15.1**	**-149**	**-1.0**	**-63**	**-1.0**	**-63**	**-16.2**	**-154**
25	**-14.6**	**-163**	**-1.1**	**-81**	**-1.1**	**-81**	**-15.9**	**-176**
26	**-15.3**	**-178**	**-1.2**	**-99**	**-1.2**	**-99**	**-15.9**	**160**
27	**-16.3**	**165**	**-1.2**	**-118**	**-1.2**	**-118**	**-16.2**	**136**
28	-17.6	153	-1.3	-137	-1.3	-137	-17.0	110
29	-18.9	138	-1.4	-156	-1.4	-156	-17.1	83
30	-21.0	125	-1.5	-175	-1.4	-175	-17.9	53
31	-24.9	121	-1.5	165	-1.6	165	-18.7	15
32	-30.0	140	-1.6	145	-1.6	145	-19.7	-32
33	-23.0	-169	-1.7	125	-1.7	124	-18.1	-91
34	-16.4	-179	-1.9	103	-1.9	103	-14.4	-139
35	-12.2	163	-2.3	82	-2.3	82	-11.1	-174
36	-9.4	147	-2.8	61	-2.8	61	-8.1	159
37	-7.3	129	-3.4	41	-3.4	41	-6.5	135
38	-5.8	114	-3.9	23	-3.9	23	-5.5	117
39	-5.4	101	-4.2	7	-4.2	7	-5.3	102
40	-5.3	91	-4.0	-11	-4.0	-11	-5.5	91
41	-7.4	73	-4.5	-34	-4.4	-34	-7.2	71
42	-9.2	68	-4.3	-58	-4.4	-58	-9.8	69
43	-10.3	84	-4.7	-85	-4.7	-85	-11.6	93
44	-7.6	96	-5.7	-112	-5.7	-112	-7.3	105
45	-4.9	90	-7.1	-136	-7.0	-136	-4.4	97
46	-2.9	79	-8.8	-161	-8.7	-160	-2.6	84
47	-2.1	68	-11.0	179	-10.8	178	-1.5	71
48	-1.9	56	-12.7	163	-12.7	162	-0.9	56
49	-1.8	48	-14.4	142	-14.3	141	-0.9	41
50	-2.0	40	-16.8	123	-16.8	123	-1.5	28

Refer to the “definition of the Sij reference planes” section below.

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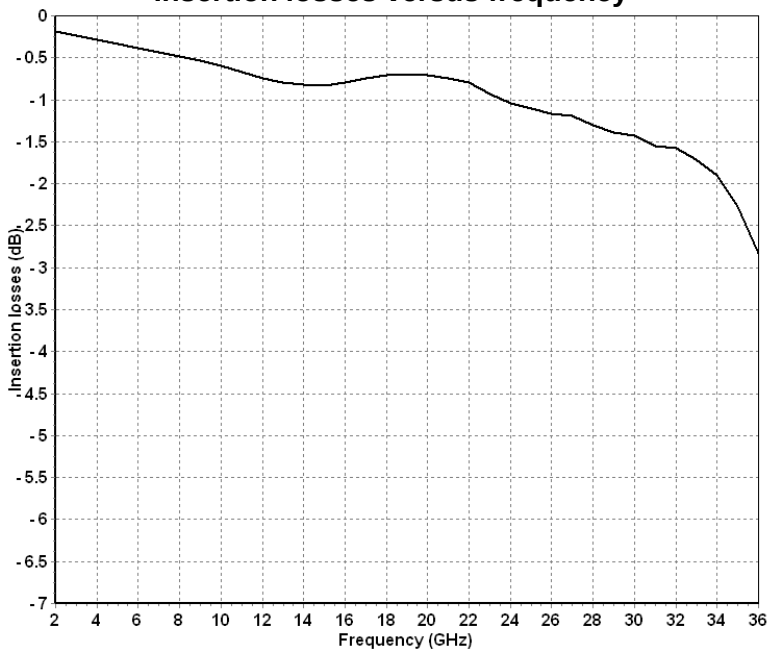
Typical Measured Performance

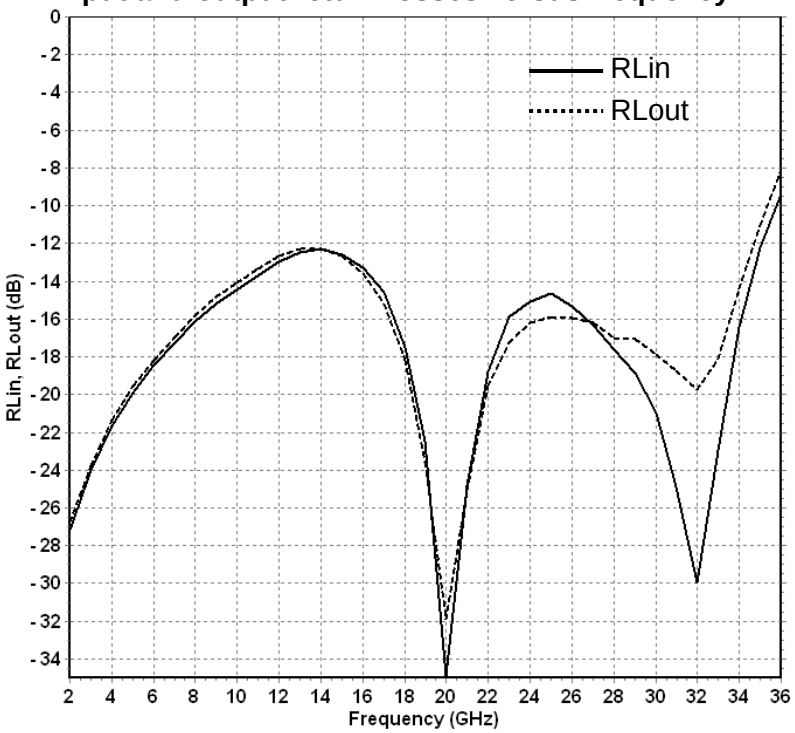
Tamb = +25°C, Vdc = +4.5V (on DC_I and DC_R), 100kΩ resistor in parallel on pads Vdet_I, Vref_I, Vdet_R and Vref_R (see notes).

Losses measurements in the package access plans
(refer to the “definition of the Sij reference planes” section below)

Insertion losses versus frequency



Input and output return losses versus frequency



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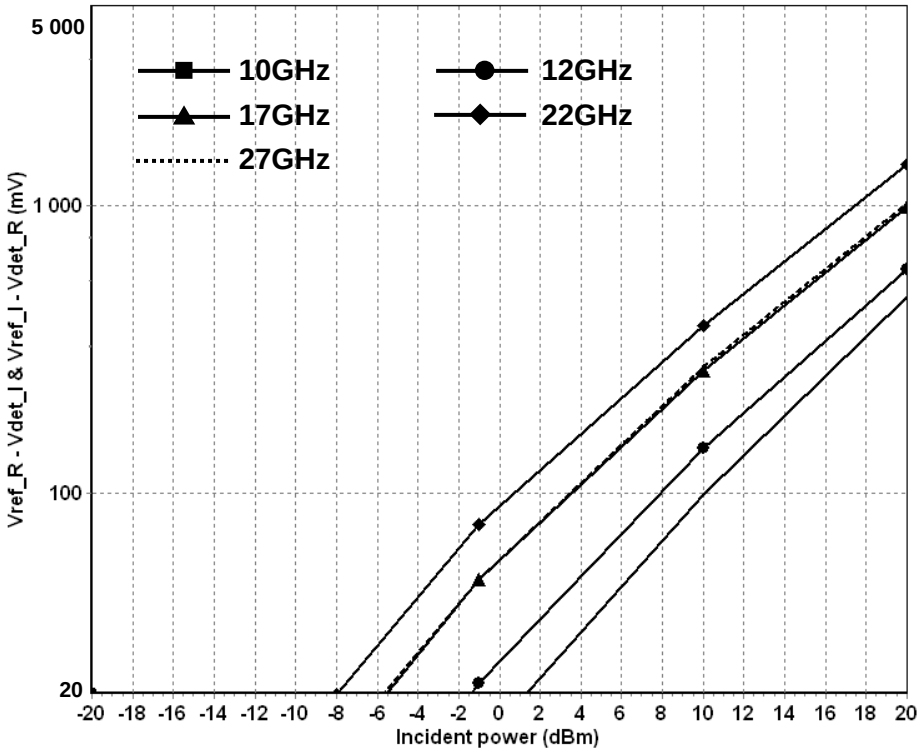
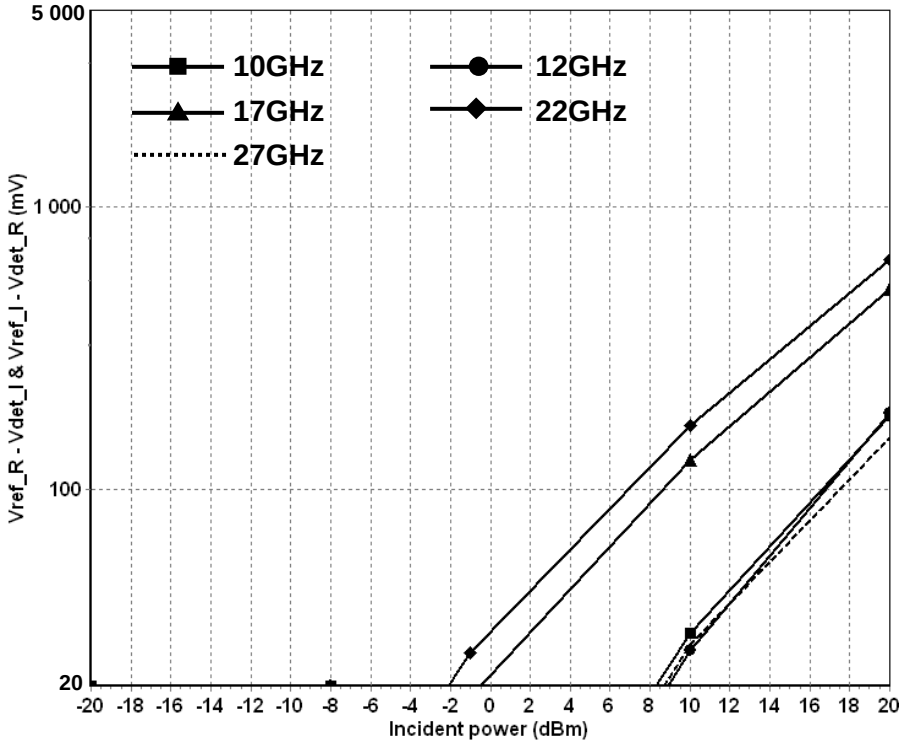
Power measurements in the plan of the connectors
using the proposed land pattern in paragraph "Evaluation mother board"

Incident power detection versus incident power @ different frequencies (Vdetect_I)



Reflected power detection versus incident power @ different frequencies (Vdetect_R)



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Typical Measured Performance: Notes

The CHE1260-QAG is a bidirectionnal detector using a symmetrical bidirectionnal coupler. Therefore the incident power detection versus incident power is identical to the reflective power detection versus reflected power.

The reflective power detection versus incident power depends on both the coupler directivity and the reflective environment of the package.

The following typical measured performances are obtained for a packaged detector, assembled on a connectorized board.

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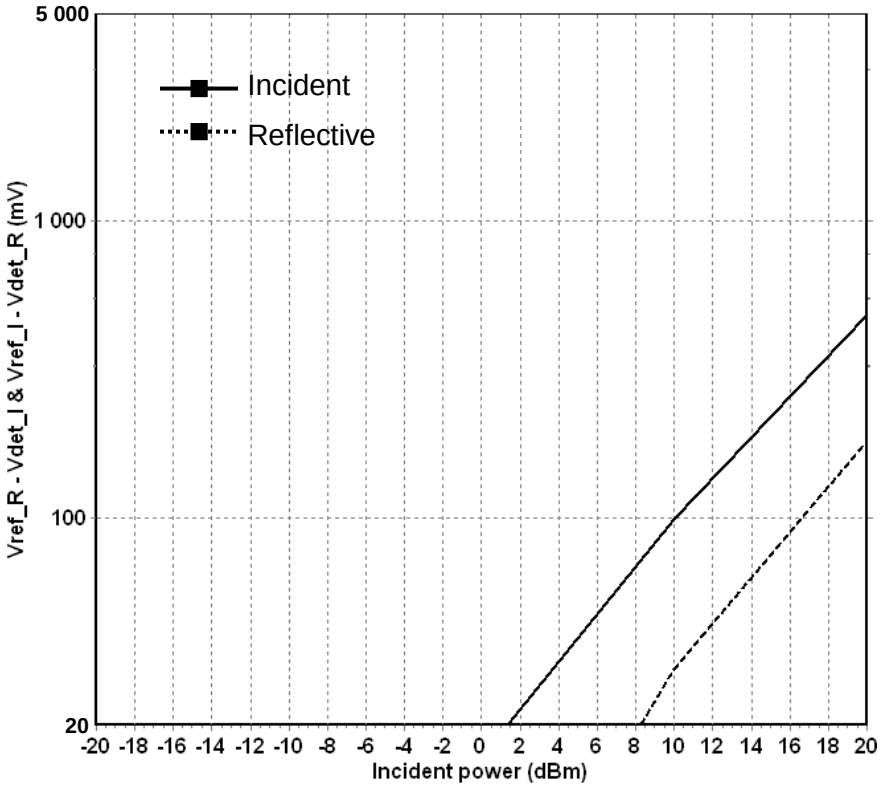
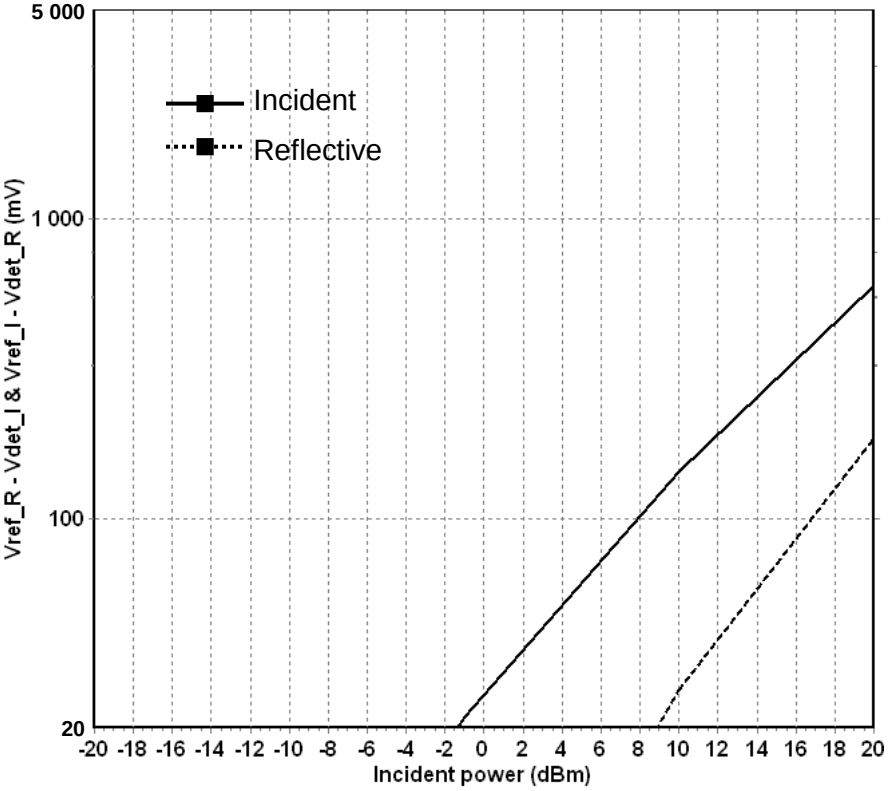
Incident and reflective power detection versus incident power @ 10GHz (Vdetect_I & Vdetect_R)



Incident and reflective power detection versus incident power @ 12GHz (Vdetect_I & Vdetect_R)



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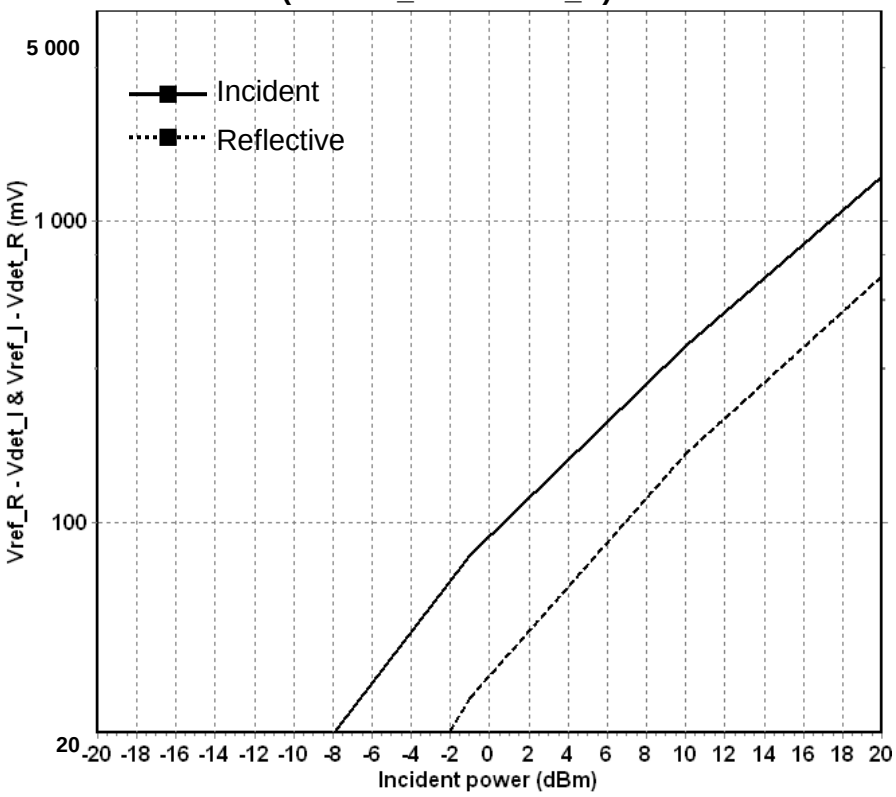
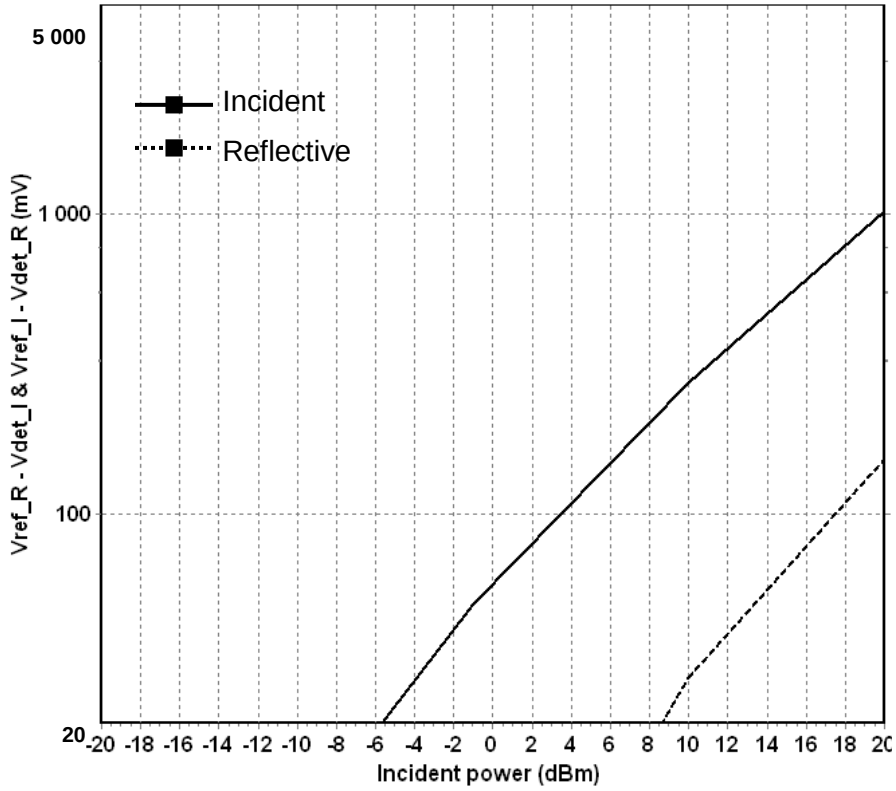
(Vdetect_I & Vdetect_R)



Incident and reflective power detection versus incident power @ 27GHz
(Vdetect_I & Vdetect_R)



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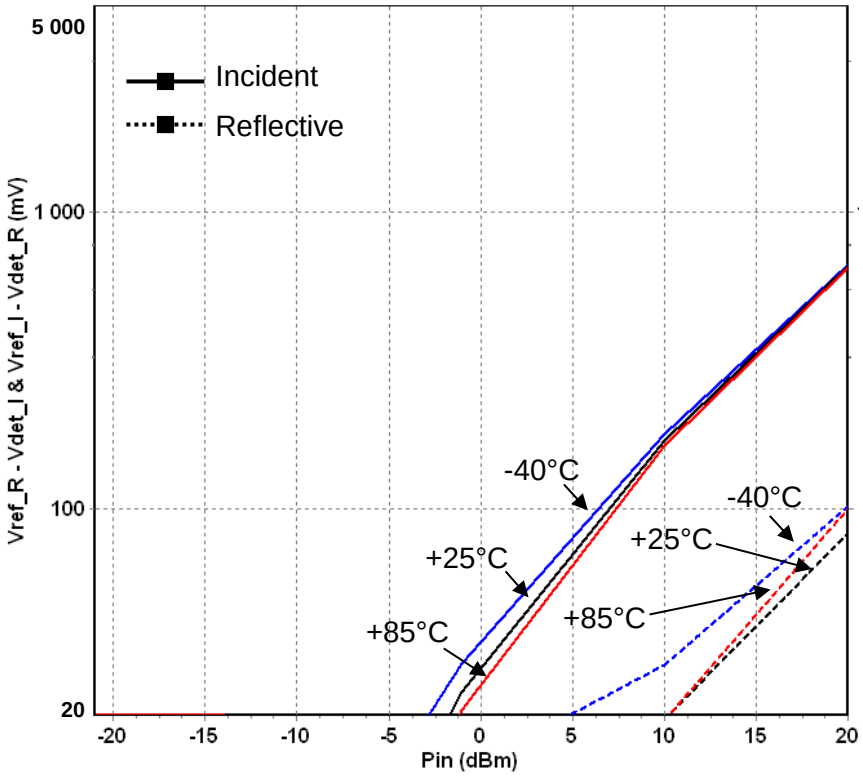
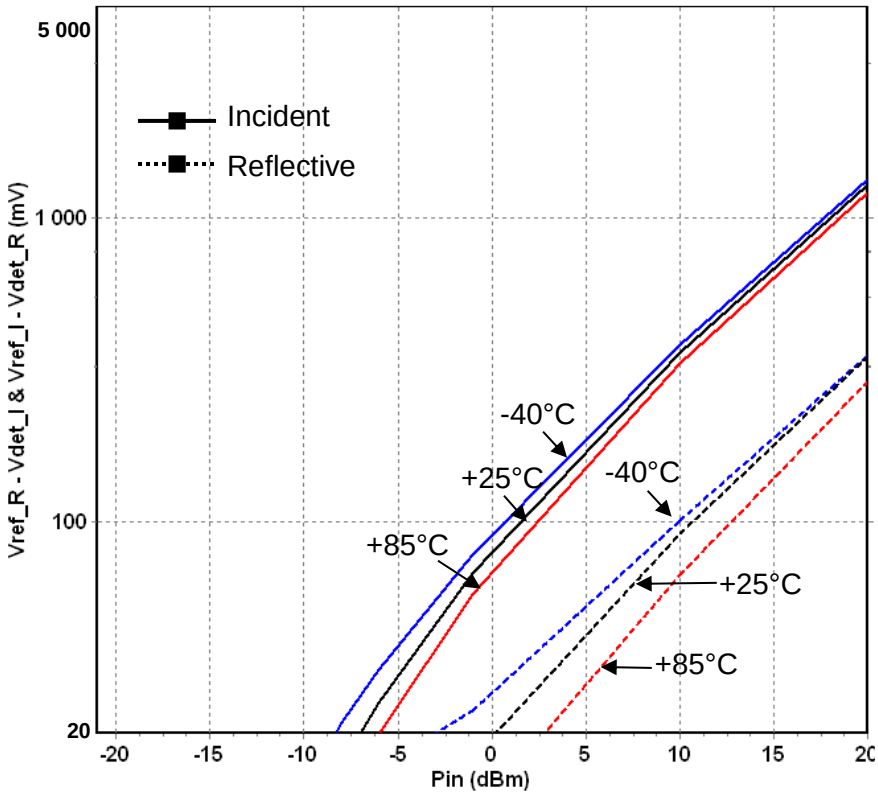
Incident and reflective power detection versus incident power and temperature @ 12GHz (Vdetect_I & Vdetect_R)



Incident and reflective power detection versus incident power and temperature @ 22GHz (Vdetect_I & Vdetect_R)



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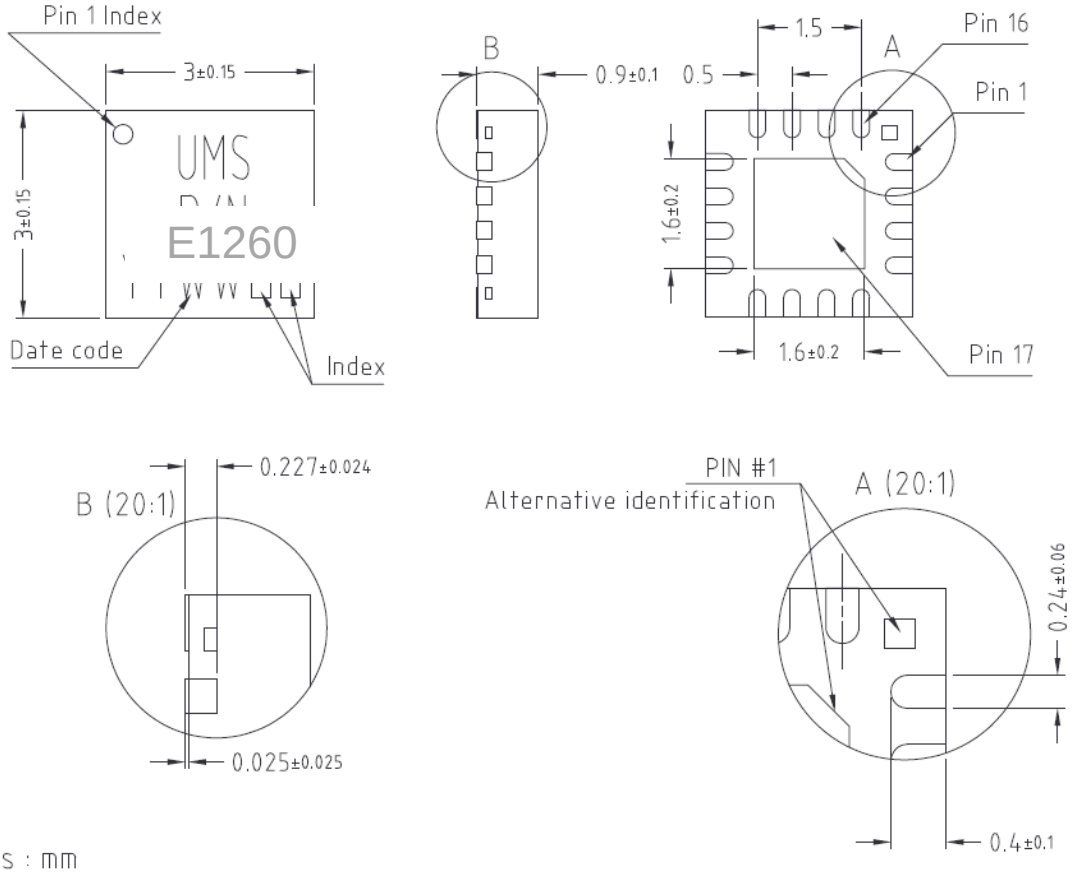
Package outline [1]:



Units : mm
From the standard : JEDEC MO-220 [VEED]
Matt tin, Lead free (Green)

Matt tin, Lead Free	(Green)	1-	Nc	9-	Gnd
Units	mm	2-	Gnd	10-	RF OUT
From the standard	JEDEC MO-220	3-	RF IN	11-	Gnd
	(VEED)	4-	Gnd	12-	Nc
17- GND		5-	DET_I	13-	Nc
		6-	DC_I	14-	DET_R
		7-	REF_I	15-	DC_R
		8-	Nc	16-	REF_R

[1]The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at https://www.ums-rf.com for exact package dimensions.
It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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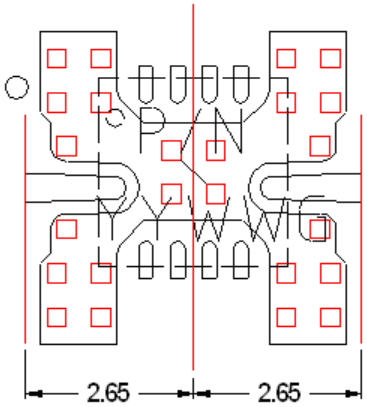
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 2.65mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the recommended land pattern of the evaluation motherboard.



Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at https://www.ums-rf.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

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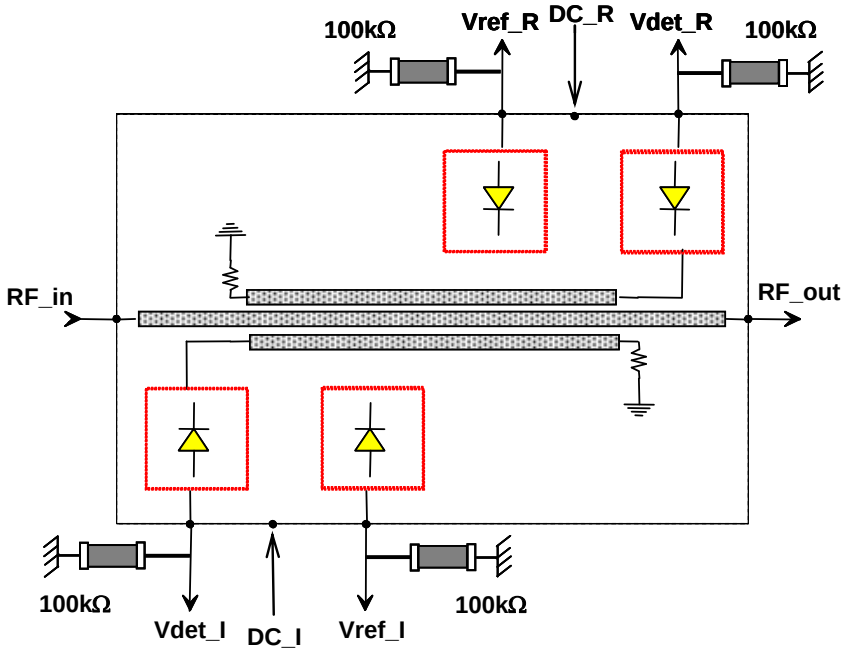
Notes



Recommended external resistors assembly

100kΩ resistors in parallel with Vdet_I, Vref_I, Vdet_R and Vref_R pads are recommended to provide the best behaviour in the whole operating temperature range.

Best accuracy is obtained when:

Vdetect_ I= Vref_R- Vdet_I

Vdetect_R= Vref_I- Vdet_R

As the voltage detection is the difference between Vref_X and Vdet_X (X= I or R), the external resistor value should be identical on these ports.
For information, a variation of 2% leads around 1mV variation of detected voltage.

ESD protections are implemented on Vdet_I, Vref_I, Vdet_R and Vref_R accesses.

The DC connections (DC_R & DC_I) do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

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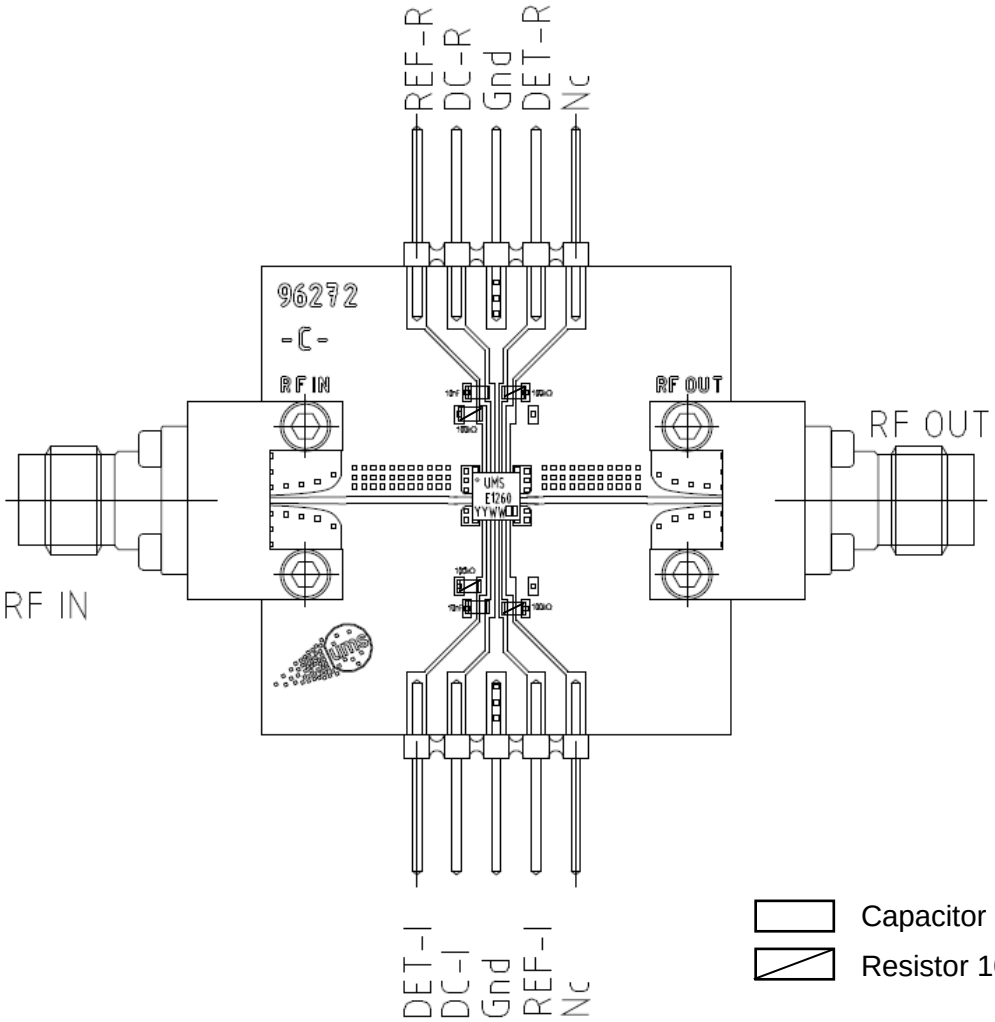
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



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Ordering Information

QFN 3x3 RoHS compliant package: CHE1260-QAG/XY

Stick: XY = 20 Tape & reel: XY = 21

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