CHA6652-98F

21-27.5GHz Power Amplifier

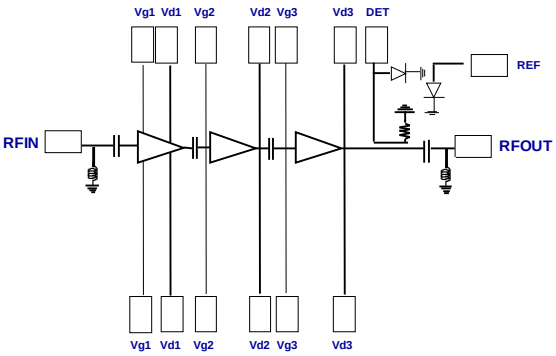
GaAs Monolithic Microwave IC bare die

Description

The CHA6652-98F is a three stage monolithic GaAs High Power Amplifier circuit producing 2W output power. It integrates differential mode power detector at the output. Gain control up to 15dB is achievable thanks to gate voltage.

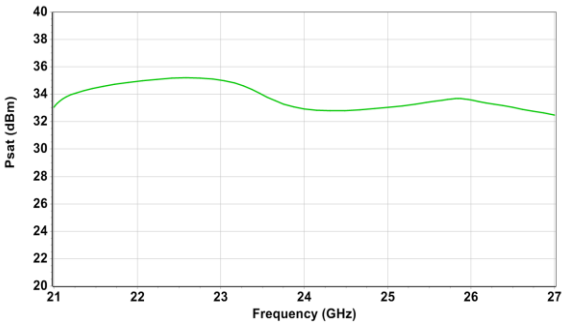
It is a field proven solution for Point to Point telecommunication systems. The circuit is highly linear and compatible with the last generation of Digital Pre-Distortion. Its versatile biasing condition helps to tune the performances.

The circuit is manufactured with an internal pHEMT space evaluated process, 0.15µm gate length.



Main Features

- Broadband performances: 21-27.5GHz
- 33dBm saturated power
- 39dBm OIP3
- 22.5dB gain
- Gain control up to 15dB
- DC bias: Vd = 6.0Volt @ Id=1.3A
- Chip size 3.46x3.61x0.07 mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	21		27.5	GHz
Gain(1)	Linear Gain		22.5		dB
Psat	Saturated output power		33		dBm
OIP3	Output IP3		39		dBm

(1) These values are representative of on-wafer measurements (pulsed mode) that are made without bonding wires at the RF ports.

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Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	21		27.5	GHz
Gain(1)	Small Signal Gain in 21 - 24GHz Small Signal Gain in 24.25 - 27.5GHz		23.5 22.5		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
Psat	Saturated Output Power in 21 - 24GHz Saturated Output Power in 24.25 - 27.5GHz		34.5 33		dBm
OIP3	Output IP3		39		dBm
PAE	PAE at saturation in 21 - 24GHz PAE at saturation in 24.25 - 27.5GHz		25 18		%
CG	Gain control range		15		dB
NF	Noise figure		4.5		dB
Rlin(1)	Input Return Loss		16.5		dB
Rlout(1)	Output Return Loss		23		dB
Dr	Detection dynamic range (for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF}- V_{DET} up to Psat		10 to 1500		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		1.3		A

(1) These values are representative of on-wafer measurements (pulsed mode) that are made without bonding wires at the RF ports.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8	V
Id	Drain bias quiescent current	1600	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum Input Power	+15	dBm
Tj	Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd1	DC Drain voltage 1st stage	6	V
Vd2	DC Drain voltage 2nd stage	6	V
Vd3	DC Drain voltage 3rd stage	6	V
Vg1	DC Gate voltage 1st stage	-0.65	V
Vg2	DC Gate voltage 2nd stage	-0.65	V
Vg3	DC Gate voltage 3rd stage	-0.65	V

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Typical on-wafer Sij parameters (Pulsed mode)

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA, Pulse width = 25µs, Duty cycle = 10%

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.140	175.0	-66.840	-1.3	-66.880	-164.9	-0.140	173.7
2	-0.180	169.8	-79.370	-60.8	-83.360	92.7	-0.180	167.9
3	-0.200	164.4	-71.560	-18.3	-62.530	-34.0	-0.170	161.5
4	-0.260	158.5	-75.720	-45.0	-69.120	20.2	-0.220	154.8
5	-0.350	152.2	-68.230	-151.1	-61.380	25.9	-0.320	148.1
6	-0.520	144.5	-75.440	125.9	-49.370	-48.8	-0.500	140.4
7	-0.940	135.2	-71.850	170.4	-44.100	-131.5	-0.810	131.7
8	-1.740	125.8	-73.130	147.5	-44.210	152.5	-1.370	122.4
9	-3.790	120.4	-73.840	-90.9	-41.120	61.6	-1.990	116.9
10	-4.050	126.1	-61.800	-168.1	-46.290	9.0	-2.140	109.9
11	-3.350	118.0	-57.700	149.0	-42.820	-43.1	-2.360	99.2
12	-3.690	103.5	-53.390	131.0	-46.230	-166.9	-2.720	86.3
13	-4.980	83.0	-54.370	103.3	-55.600	131.2	-3.190	67.7
14	-8.840	53.8	-58.710	132.9	-55.270	95.4	-4.800	40.7
15	-24.480	14.4	-55.120	112.2	-55.120	131.9	-9.210	6.0
16	-15.030	162.7	-48.580	58.8	-28.410	-127.4	-22.880	-5.0
17	-12.990	128.7	-48.200	32.6	-0.430	121.6	-17.140	64.9
18	-17.310	133.9	-47.600	11.9	16.270	-44.4	-17.030	37.9
19	-12.730	147.0	-47.440	-41.3	22.810	162.3	-20.850	-26.1
20	-14.570	120.4	-55.220	-105.5	23.480	28.4	-26.270	-9.0
21	-18.110	133.4	-55.380	-151.8	23.180	-73.8	-27.080	-62.3
22	-13.570	140.7	-51.250	153.6	23.620	-169.2	-24.380	178.3
23	-15.360	98.6	-55.310	108.1	24.110	96.7	-27.610	59.8
24	-23.120	136.5	-61.790	89.3	24.150	0.3	-34.680	-24.0
25	-18.410	161.3	-45.330	127.6	23.240	-94.1	-28.400	-93.5
26	-14.640	111.1	-47.870	96.5	22.350	169.2	-26.180	63.1
27	-21.680	-0.8	-46.640	114.5	22.230	72.3	-15.620	-36.2
28	-15.040	127.0	-37.650	49.6	21.780	-89.9	-31.790	108.6
29	-18.090	39.5	-39.490	27.6	7.130	152.1	-18.810	-55.0
30	-18.190	-15.9	-39.090	-14.8	-4.870	73.6	-21.650	-37.5
31	-17.060	-72.1	-42.070	-42.6	-14.320	8.3	-15.530	-25.7
32	-19.270	-118.1	-42.010	-61.7	-24.110	-38.4	-11.470	-50.5
33	-25.530	173.6	-44.940	-92.8	-29.210	-93.8	-9.700	-75.7
34	-16.550	48.2	-49.090	-106.3	-34.280	-129.8	-11.190	-99.1
35	-9.280	-4.2	-48.620	-152.8	-45.140	107.6	-16.290	-109.0
36	-6.140	-39.5	-54.000	164.0	-39.010	-177.8	-16.250	-41.8
37	-5.080	-63.8	-59.260	108.8	-46.760	-155.1	-10.930	-49.2
38	-4.830	-81.0	-53.950	51.6	-42.700	23.5	-8.290	-50.4
39	-4.330	-92.0	-42.930	140.4	-42.400	100.6	-4.830	-70.9
40	-4.160	-108.2	-40.250	85.7	-37.190	47.0	-4.330	-91.9

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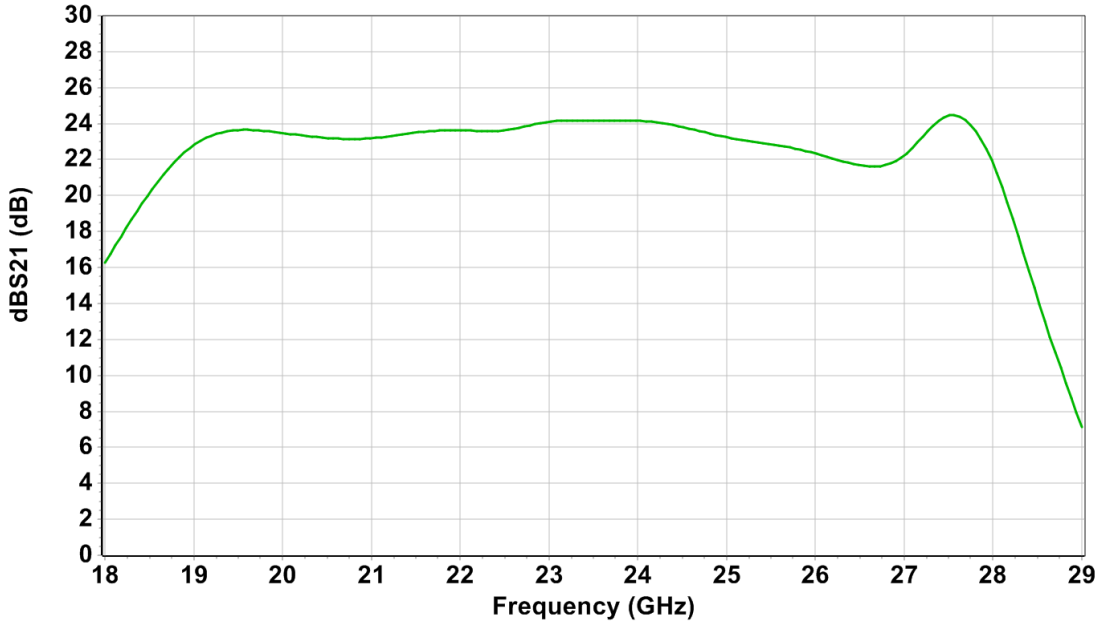
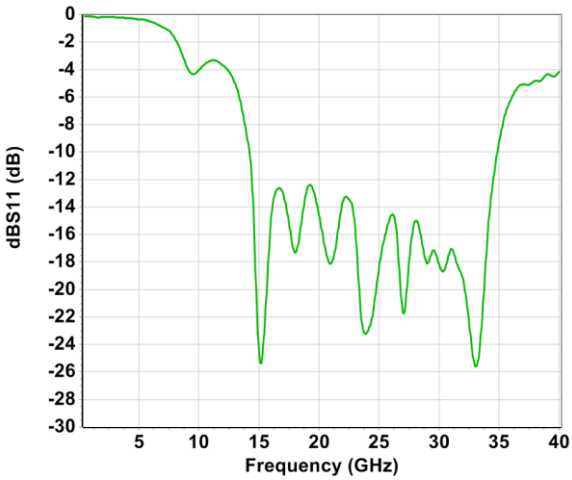
Typical on-wafer Sij Measurements (Pulsed mode)

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA, Pulse width = 25µs, Duty cycle = 10%
Measurement performed in the access plans of the die.

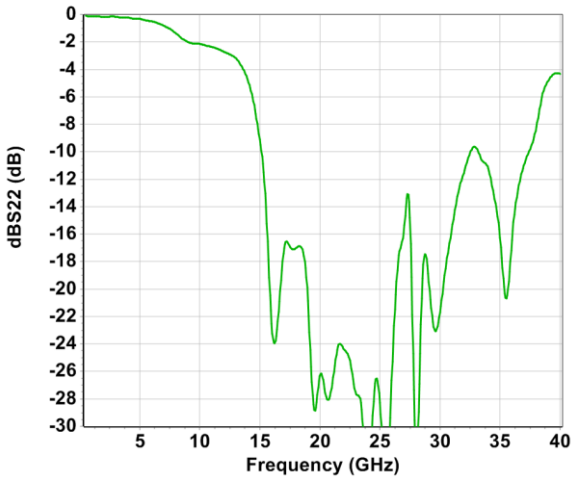
Linear Gain versus Frequency



Input Return Loss versus Frequency



Output Return Loss versus Frequency



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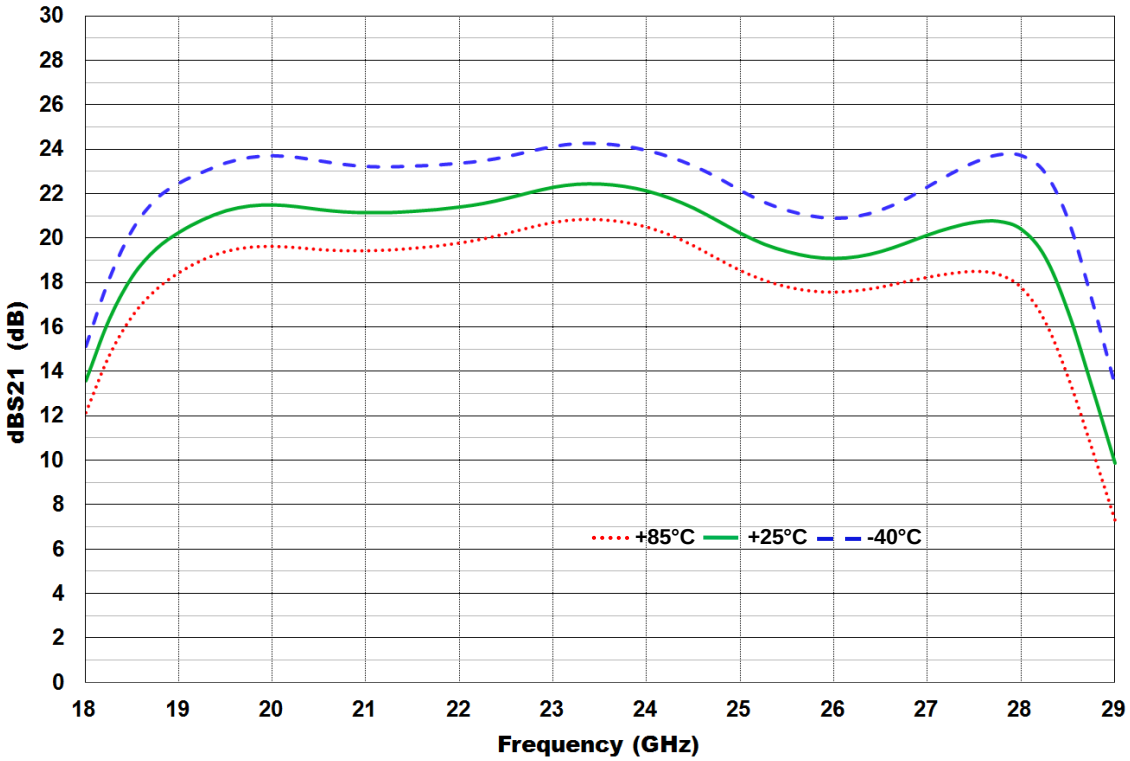
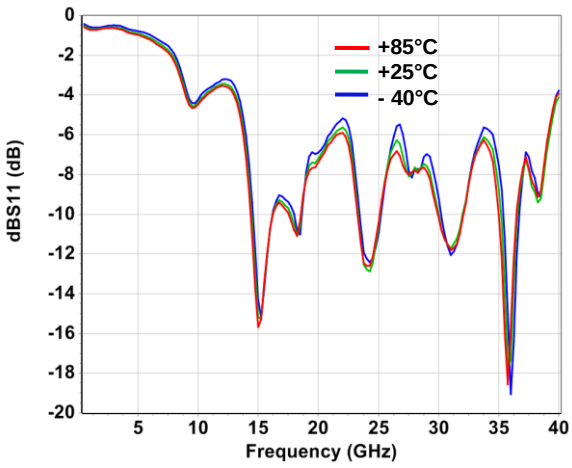
Typical Board Measurements (CW mode)

Vd = +6.0V, Id = 1300mA
Measurement performed in the access plans of the connectors, using the proposed board as defined in paragraph “Evaluation mother board”. Board losses have been taken into account to plot all the following measurements below.

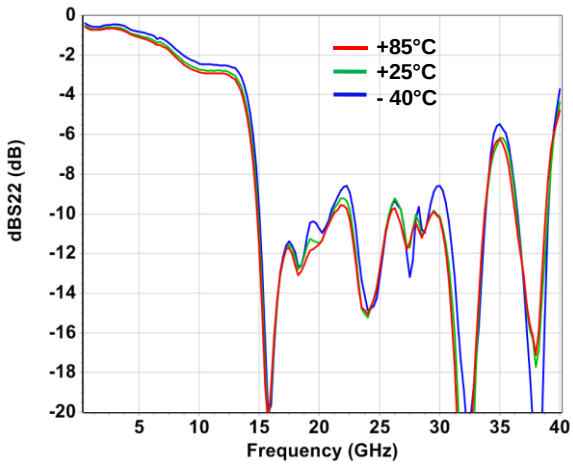
Linear Gain versus Frequency in Temperature



Input Return Loss versus Frequency in Temperature



Output Return Loss versus Frequency in Temperature



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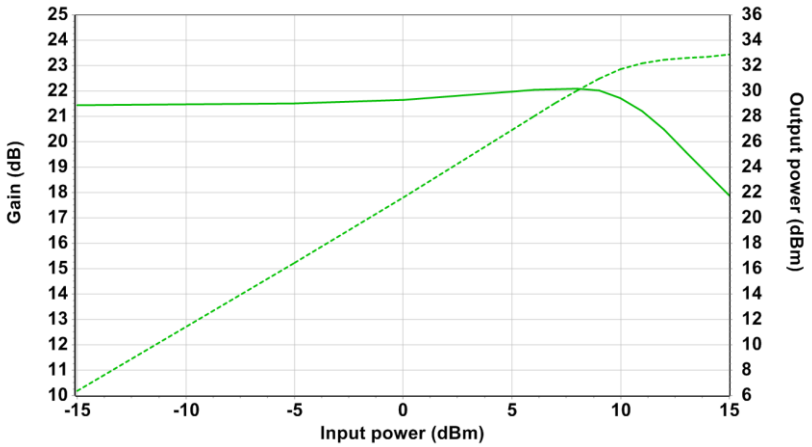
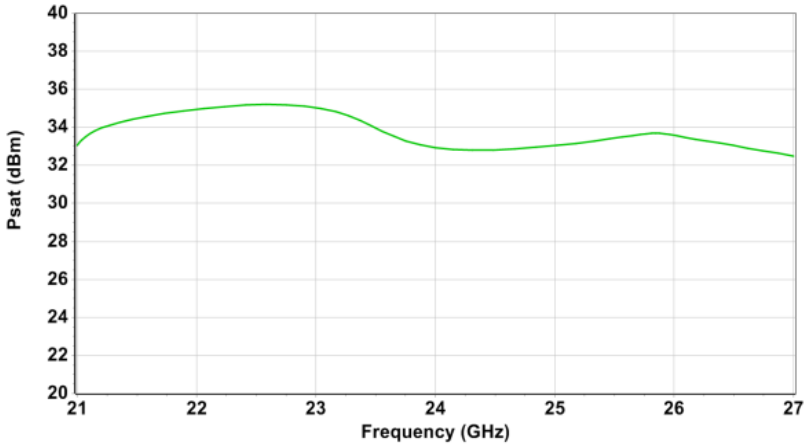
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

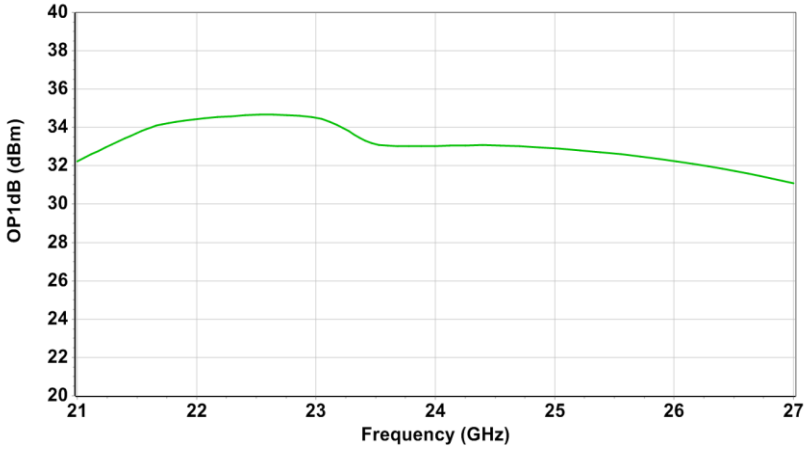
Gain & Output Power versus Input Power at 24GHz



Saturated Power versus Frequency



Output Power at 1dB compression versus Frequency



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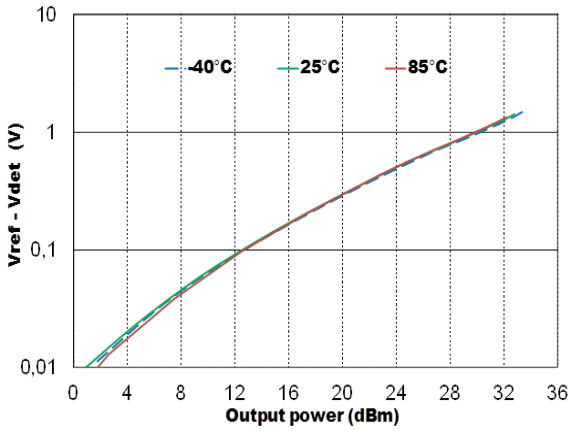
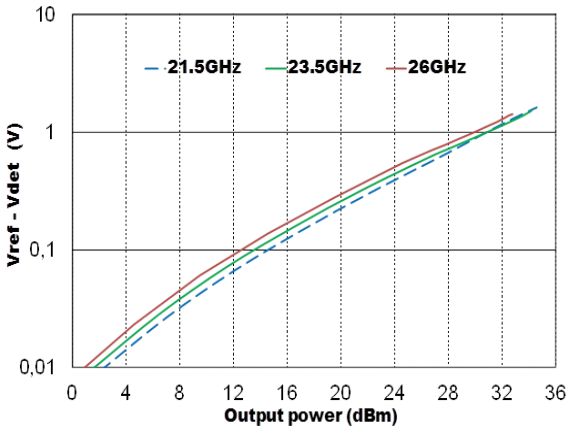
Typical Board Measurements (CW mode)

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

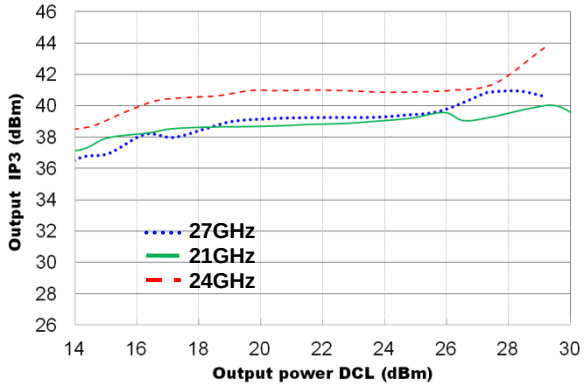
Power Detector versus Pout and Temperature

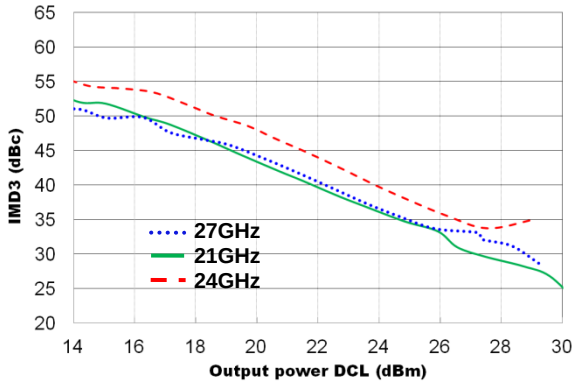


Power Detector versus Pout and Frequency

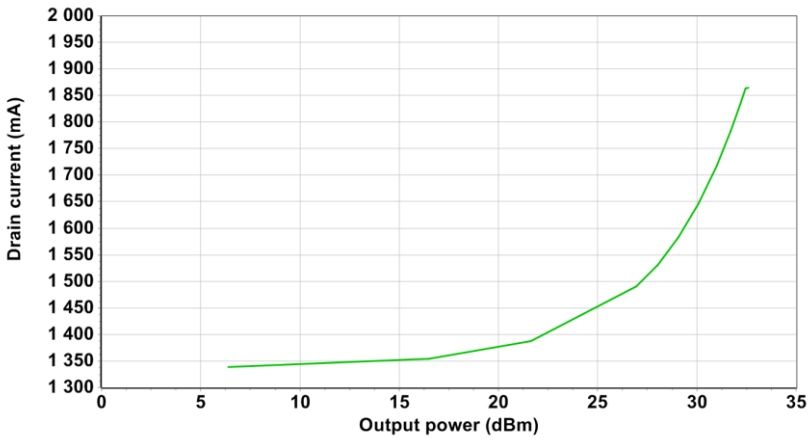


Output IP3 and IMD3 versus Output Power DCL and Frequency





Total Drain Current versus Output Power at 24GHz



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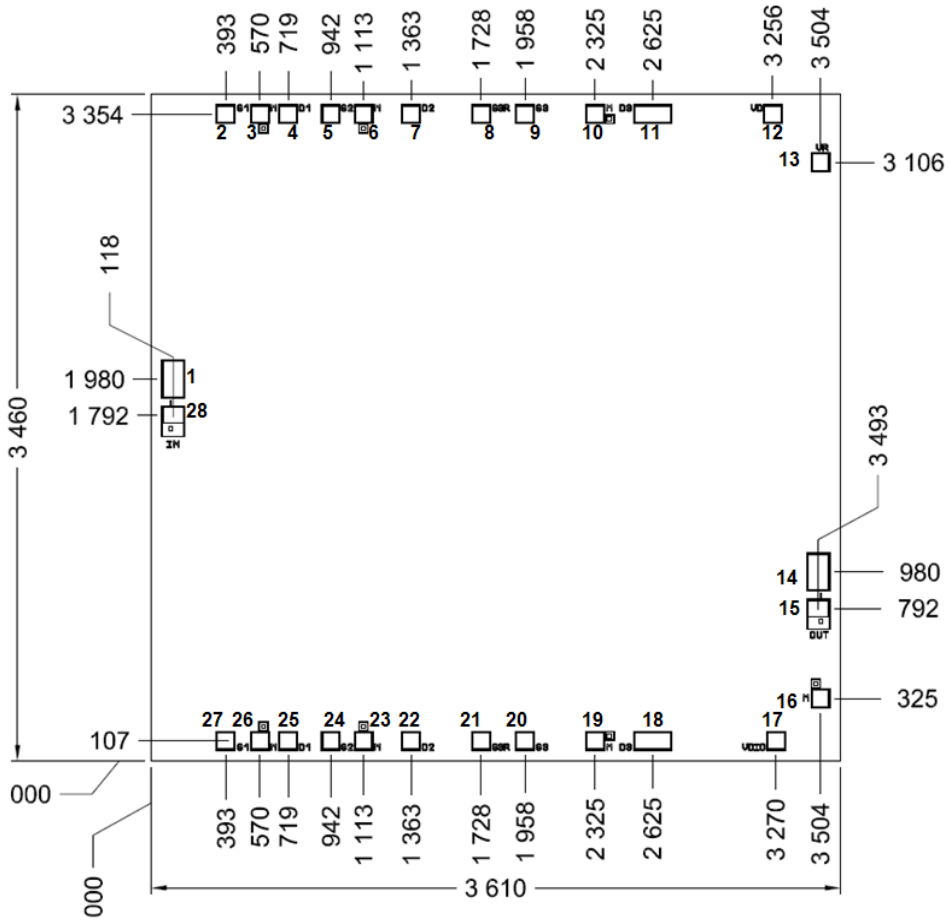
Mechanical data



Chip thickness: 70µm.
All dimensions are in micrometers
DC pad size: 83um x 83 um (BCB opening)
RF pad size: 90um x 180 um (BCB opening)

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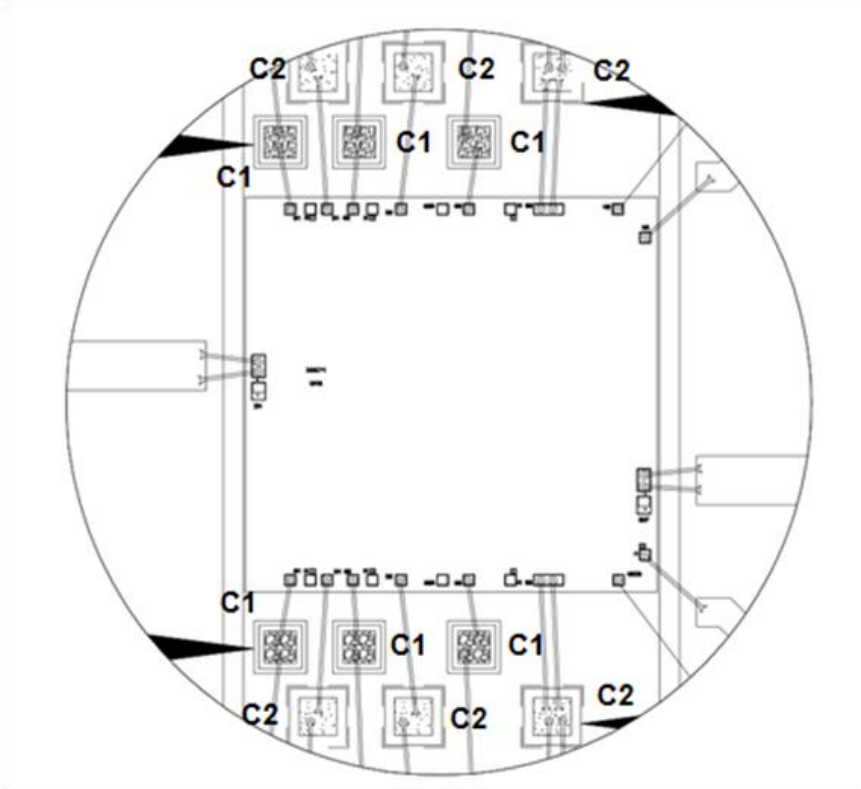
Recommended assembly plan



C1=22pF (on gate access) & C2=120pF (on drain access)

PAD Number	Name	Description
1	RF IN	Input RF port
14	RF OUT	Output RF port
2, 27	Vg1	DC Gate voltage 1st stage(1)
4, 25	Vd1	DC Drain voltage 1st stage(1)
5, 24	Vg2	DC Gate voltage 2nd stage(1)
7, 22	Vd2	DC Drain voltage 2nd stage(1)
9, 20	Vg3	DC Gate voltage 3rd stage(1)
11, 18	Vd3	DC Drain voltage 3rd stage(1)
12	DET	Voltage detection
13	REF	Voltage reference

(1) Connect the both pads is mandatory

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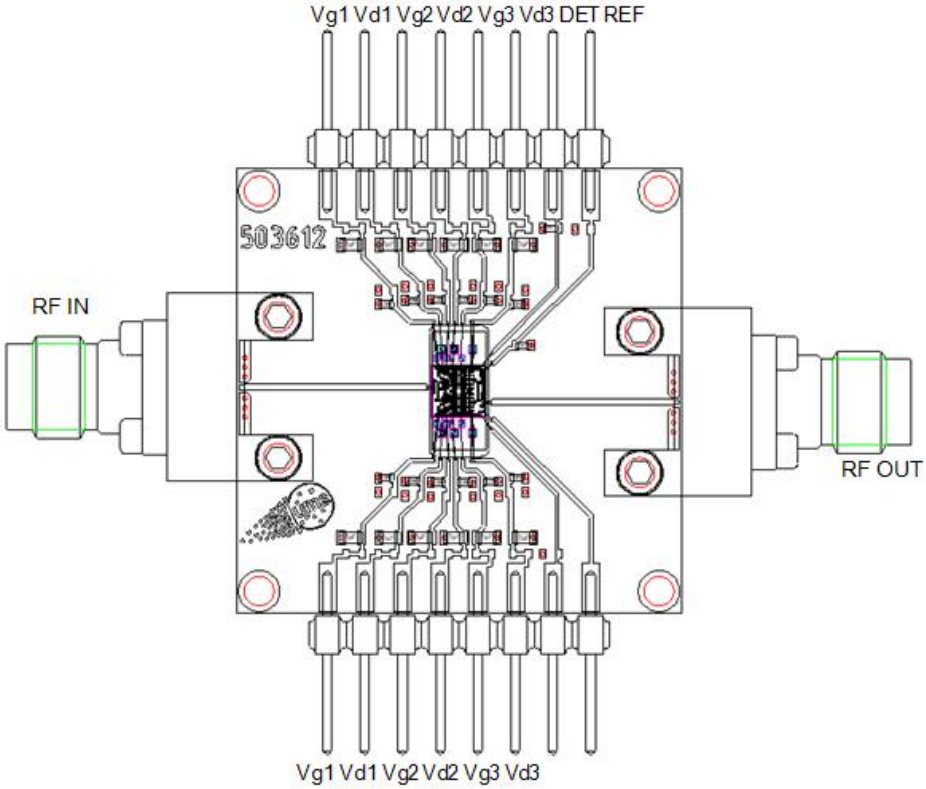
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003C / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the chip.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 22pF ±10%, 10nF ±10% and 1µF ±10% are recommended for the gate accesses.
- Decoupling capacitors of 120pF ±10%, 10nF ±10% and 1µF ±10% are recommended for the drain accesses.
- A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



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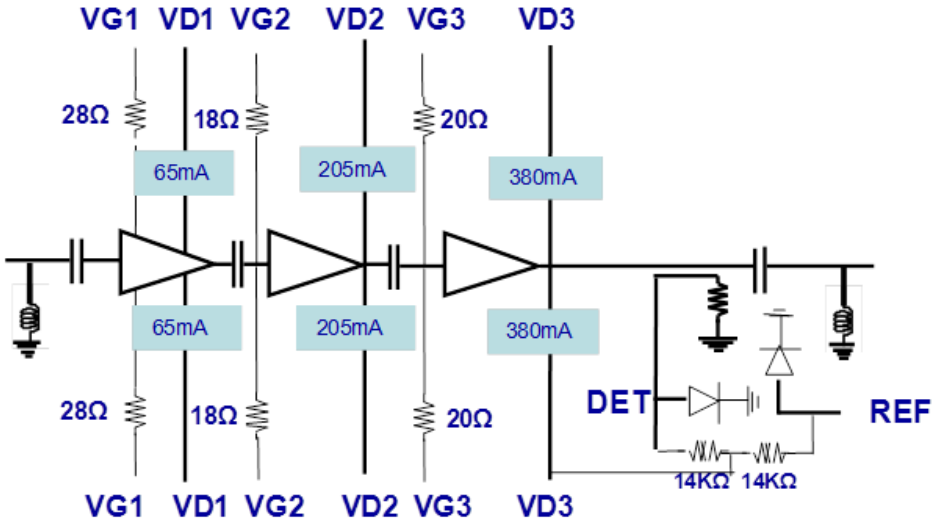
DC Schematic

HPA: 6V, 1.3A



Biasing procedure

Device Power Up instructions:

1. Ground the device
2. Bias HPA gate voltage at Vgs close to Vpinch-off (example: Vgs ≈ -2V)
3. Apply Vds quiescent bias voltage (Example: Vd = 6V)
4. Increase slowly Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
5. Apply RF input power

Device Power Down instructions:

1. Remove RF input power
2. Decrease HPA gate voltage down to Vgs -2V
3. Decrease drain voltage down to 0V

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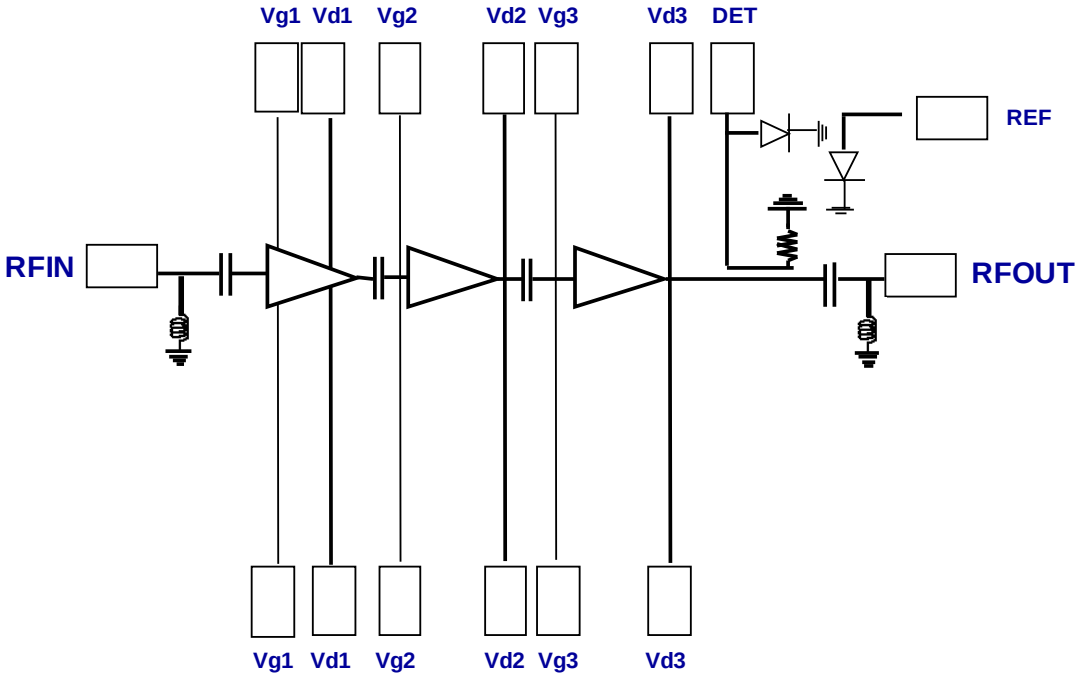
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor, therefore it is mandatory to provide a good external DC decoupling (22pF, 120pF, 10nF, 1µF) on the PC board, as close as possible to the bare die.

A 10kΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC accesses.

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Bare Die:	CHA6652-98F/00

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