

## 6-16GHz Low Noise Amplifier

### GaAs Monolithic Microwave IC in SMD package

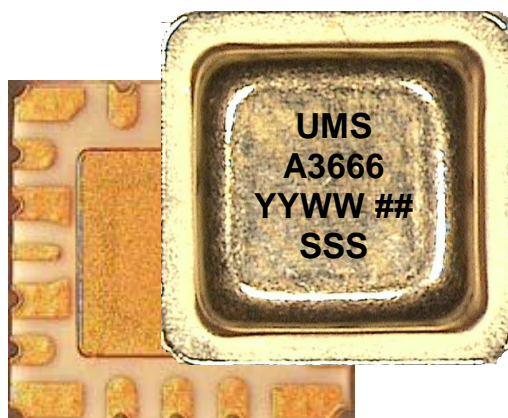
#### Description

The CHA3666-FAB is a two-stage self-biased wide band monolithic Low Noise Amplifier.

The circuit is manufactured with a standard pHEMT process: 0.25 $\mu$ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

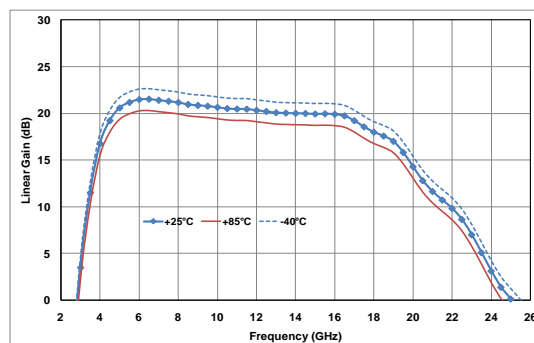
It is proposed in leadless surface mount hermetic metal ceramic 6x6mm<sup>2</sup> package. The overall power supply is of 4V/80mA.

The circuit is dedicated to space applications and also well suited for a wide range of microwave and millimetre wave applications and systems.



#### Main Features

- Broadband performance 6-16GHz
- 1.8dB typical Noise Figure
- 24dBm 3<sup>rd</sup> order intercept point
- 16dBm power at 1dB compression
- 21dB gain
- Low DC power consumption
- 6x6mm<sup>2</sup> metal ceramic hermetic package



#### Main Electrical Characteristics

T<sub>amb.</sub> = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		16	GHz
NF	Noise figure		1.8	2.5	dB
G	Small signal Gain	18.5	21		dB
IP3	3rd order intercept point		24		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

**Electrical Characteristics<sup>(1)</sup>**

T<sub>amb.</sub> = +25°C, V<sub>d1</sub> = V<sub>d2</sub> = +4.0V, P1 and N2 grounded, P2: NC.

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>op</sub>	Operating frequency range	6		16	GHz
G	Gain	18.5	21		dB
ΔG	Gain flatness		±1		dB
NF	Noise figure		1.8	2.5	dB
IS11I	Input return loss		7	6.5	dB
IS22I	Output return loss		10	8.5	dB
IP3	3rd order intercept point		26		dBm
P1dB	Output power at 1dB gain comp.	15	17		dBm
V <sub>d1</sub> , V <sub>d2</sub>	Drain bias voltage		4		V
I <sub>d</sub>	Drain bias current	60	80	100	mA

<sup>(1)</sup> These values are representative of on board measurements as defined on the drawing 99622 (see below).

**Absolute Maximum Ratings <sup>(1)</sup>**

T<sub>amb.</sub> = +25°C

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage (V <sub>d1</sub> & V <sub>d2</sub> )	4.5	V
P <sub>in</sub>	Maximum peak input power overdrive <sup>(4)</sup>	10	dBm
T <sub>op</sub>	Operating temperature range <sup>(2)</sup>	-40 to +85	°C
T <sub>j</sub>	Junction temperature <sup>(3)</sup>	175	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

<sup>(1)</sup> Operation of this device above any one of these parameters may cause permanent damage.

<sup>(2)</sup> T<sub>op</sub> = Package Ground Paddle back side temperature

<sup>(3)</sup> Thermal Resistance channel to ground paddle = 214°C/W for T<sub>ground paddle</sub> = +85°C

<sup>(4)</sup> Duration < 1s.

### Typical Package Sij parameters

For low current configuration in 99622 board - in connector plane

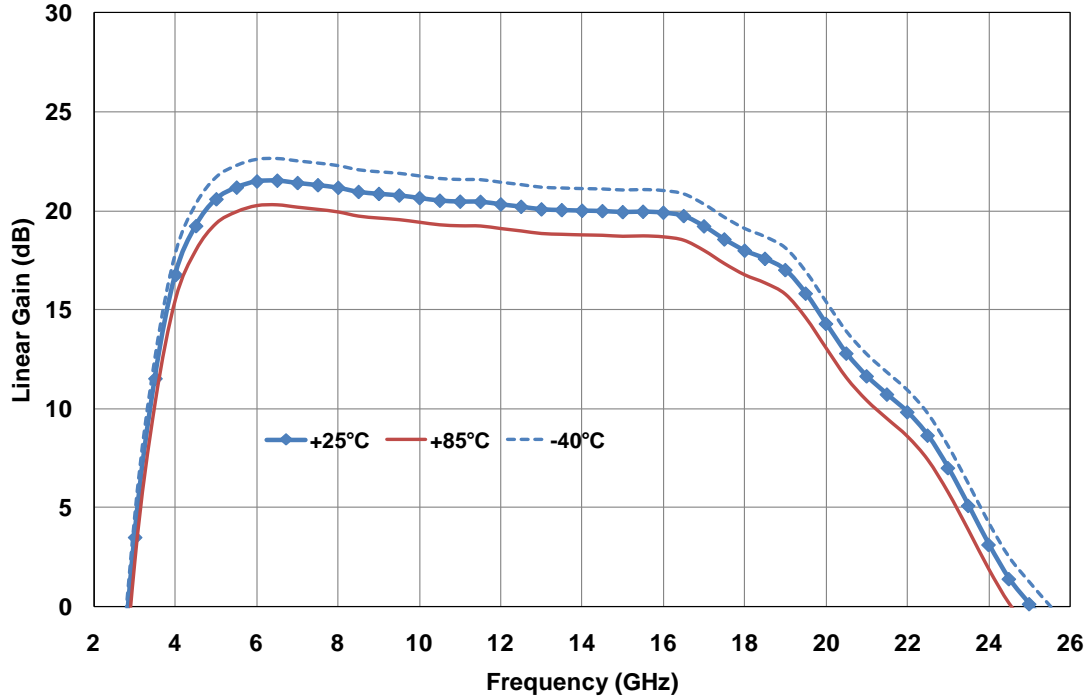
Temp = +25°C, Vd1 = Vd2 = +4.0V, P1 and N2 grounded, P2: NC, typical Id=80mA

FREQ (GHz)	dBS11	PhS11 (°)	dBS12	PhS12 (°)	dBS21	PhS21 (°)	dBS22	PhS22 (°)
1.0	-0.28	-128.50	-77.75	166.70	-51.19	155.80	-0.37	-135.00
2.0	-0.86	106.10	-65.63	41.41	-31.56	145.10	-0.89	99.75
3.0	-1.71	-35.04	-59.27	-156.30	3.47	-4.84	-4.09	-47.00
3.5	-3.19	-124.40	-66.37	123.50	11.50	-114.90	-6.81	-113.00
4.0	-6.34	127.50	-56.70	-148.20	16.74	137.80	-9.30	-169.60
4.5	-9.09	12.02	-49.61	127.20	19.21	37.78	-10.39	132.20
5.0	-10.33	-90.74	-45.83	42.90	20.57	-54.26	-11.29	76.93
5.5	-10.33	-172.60	-43.97	-31.81	21.16	-140.50	-12.62	18.97
6.0	-10.14	123.50	-42.56	-104.60	21.47	138.10	-13.32	-38.24
6.5	-10.11	66.93	-41.42	-176.30	21.51	60.52	-13.50	-103.90
7.0	-10.46	9.32	-40.56	113.20	21.39	-14.15	-12.82	-172.70
7.5	-10.69	-50.07	-40.07	44.29	21.28	-86.67	-12.01	117.50
8.0	-10.23	-109.20	-39.91	-21.61	21.15	-157.40	-11.64	48.26
8.5	-9.48	-164.80	-39.61	-86.89	20.94	133.30	-11.38	-19.82
9.0	-9.12	141.10	-39.51	-149.00	20.84	65.44	-10.84	-88.89
9.5	-9.49	85.88	-39.08	154.40	20.76	-2.64	-10.57	-155.70
10.0	-10.44	26.06	-38.25	91.93	20.63	-69.59	-10.37	144.50
10.5	-11.78	-37.75	-37.66	30.13	20.50	-136.30	-10.57	87.39
11.0	-13.07	-109.10	-37.26	-33.42	20.45	158.10	-11.81	34.84
11.5	-13.68	174.50	-37.27	-95.94	20.44	91.47	-13.46	-12.50
12.0	-13.05	103.60	-37.08	-159.30	20.31	25.43	-16.13	-62.27
12.5	-12.20	45.30	-37.12	136.70	20.19	-40.34	-20.30	-120.50
13.0	-12.10	-2.70	-37.45	73.45	20.06	-105.60	-24.41	148.00
13.5	-12.81	-48.77	-37.78	9.75	20.02	-170.90	-22.31	55.05
14.0	-14.82	-99.42	-37.93	-55.40	19.99	123.50	-21.13	-1.25
14.5	-17.05	-164.90	-38.14	-121.50	19.97	57.62	-21.82	-42.80
15.0	-17.13	119.30	-38.40	171.50	19.92	-8.40	-24.38	-83.61
15.5	-15.27	55.44	-39.04	103.10	19.94	-75.39	-33.30	-120.40
16.0	-13.15	-3.86	-39.57	36.40	19.89	-142.80	-25.55	1.44
16.5	-10.85	-65.66	-40.44	-29.32	19.72	148.50	-16.72	-51.31
17.0	-8.74	-128.80	-41.38	-100.40	19.20	79.58	-12.65	-99.21
17.5	-7.25	172.40	-43.33	-170.80	18.54	11.96	-10.18	-150.90
18.0	-6.87	116.20	-46.35	120.50	17.97	-54.40	-9.27	154.30
18.5	-7.62	55.87	-52.17	41.48	17.56	-121.90	-9.57	94.52
19.0	-8.88	-17.09	-61.92	-122.90	16.99	168.20	-10.50	24.24
19.5	-9.24	-97.74	-50.18	106.00	15.80	97.90	-11.00	-54.27
20.0	-8.52	-166.40	-45.56	38.93	14.27	30.72	-10.24	-128.70
21.0	-9.00	76.44	-40.89	-93.87	11.62	-96.01	-8.77	105.90
22.0	-12.52	-62.64	-37.85	135.90	9.80	135.20	-10.62	-20.22
23.0	-13.01	129.00	-37.52	-12.50	6.98	2.37	-12.41	169.80
24.0	-10.26	-12.31	-40.15	-127.90	3.10	-121.80	-8.67	34.13
25.0	-8.17	-120.00	-41.30	123.20	0.10	123.60	-7.07	-84.59
26.0	-7.40	128.10	-39.97	6.46	-2.23	7.45	-6.07	158.90
27.0	-6.57	14.08	-40.77	-111.10	-4.48	-105.10	-5.53	48.83
28.0	-6.56	-86.86	-40.69	131.30	-5.23	146.00	-5.49	-58.77
29.0	-8.17	151.20	-39.63	9.70	-4.25	27.54	-5.63	-166.40
30.0	-6.89	22.64	-38.52	-116.10	-3.67	-104.50	-5.39	85.11

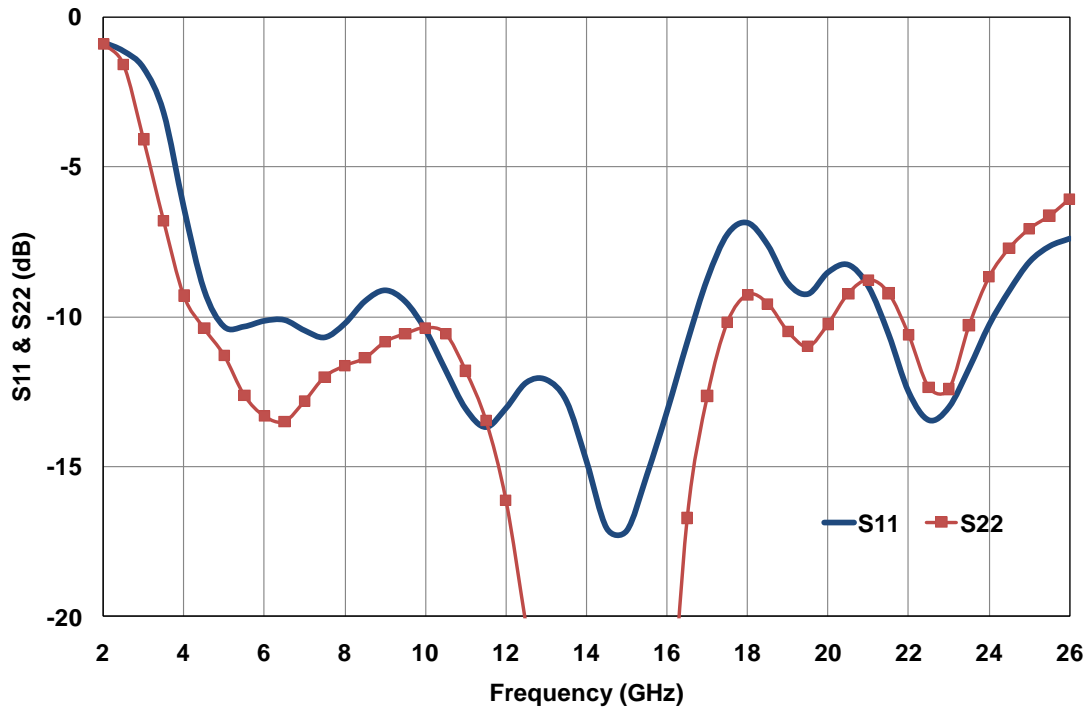
## Typical boards Measurements

Temp = +25°C, Vd1 = Vd2 = +4.0V, P1 and N2 grounded, P2: NC, typical Id=80mA  
Measurements in the connector planes, using the proposed land pattern & board 99622.

### Linear Gain versus Frequency and Temperature

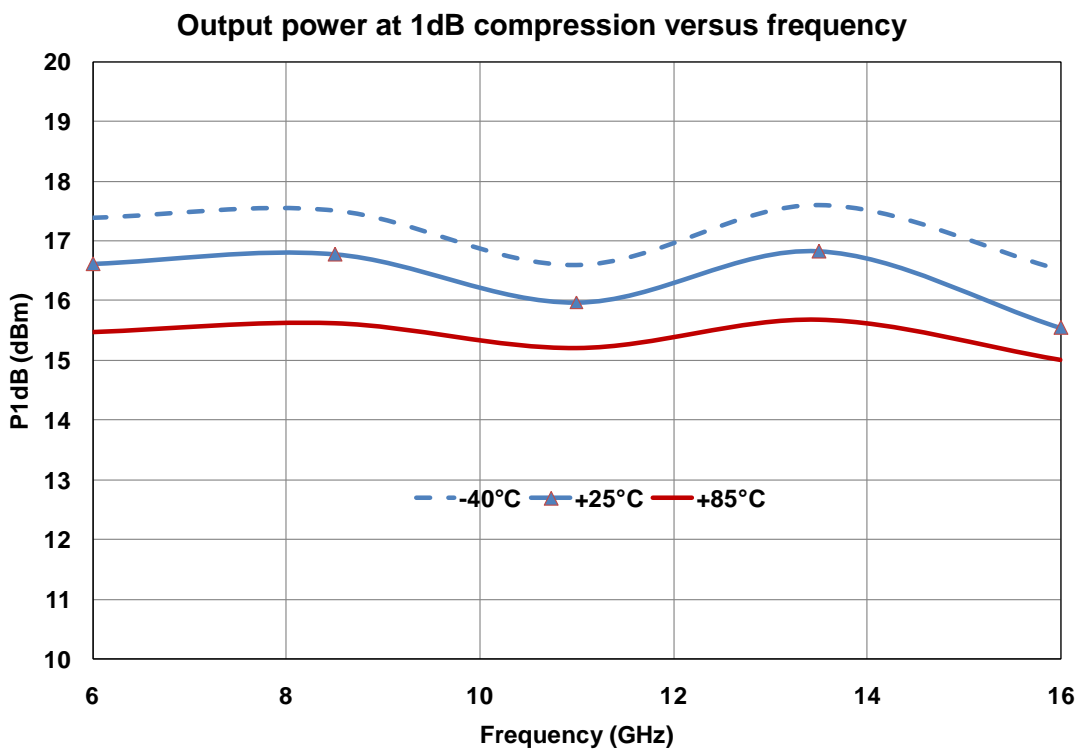
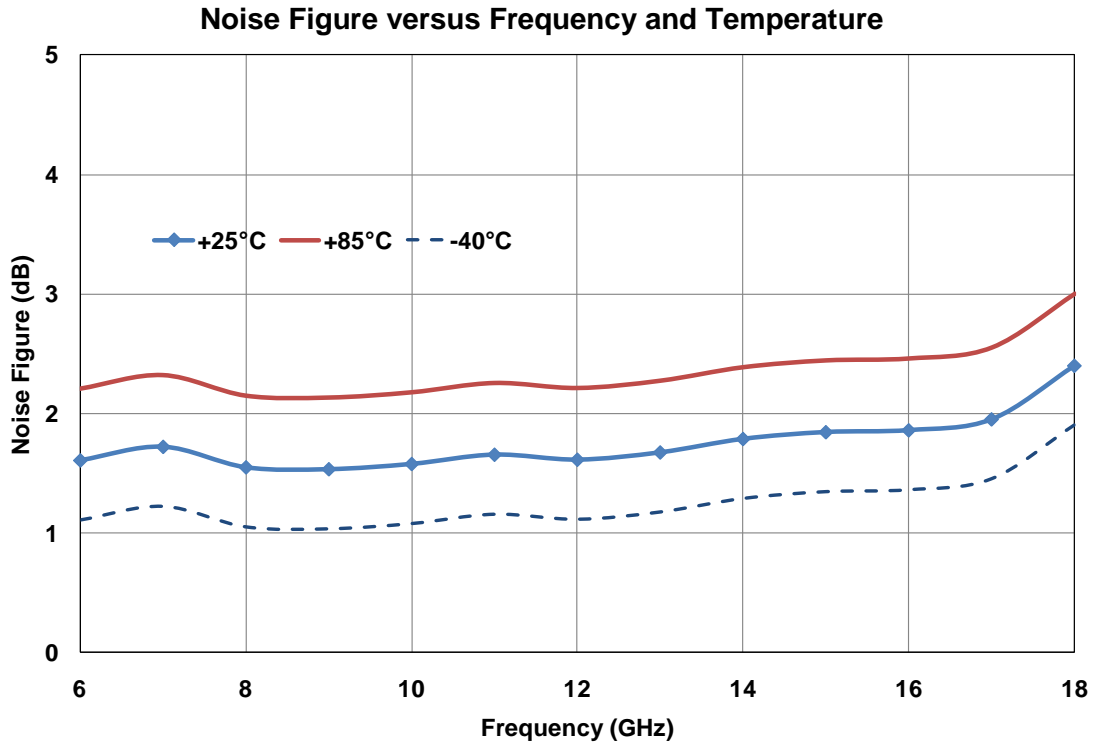


### Input & Output matching



**Typical boards Measurements**

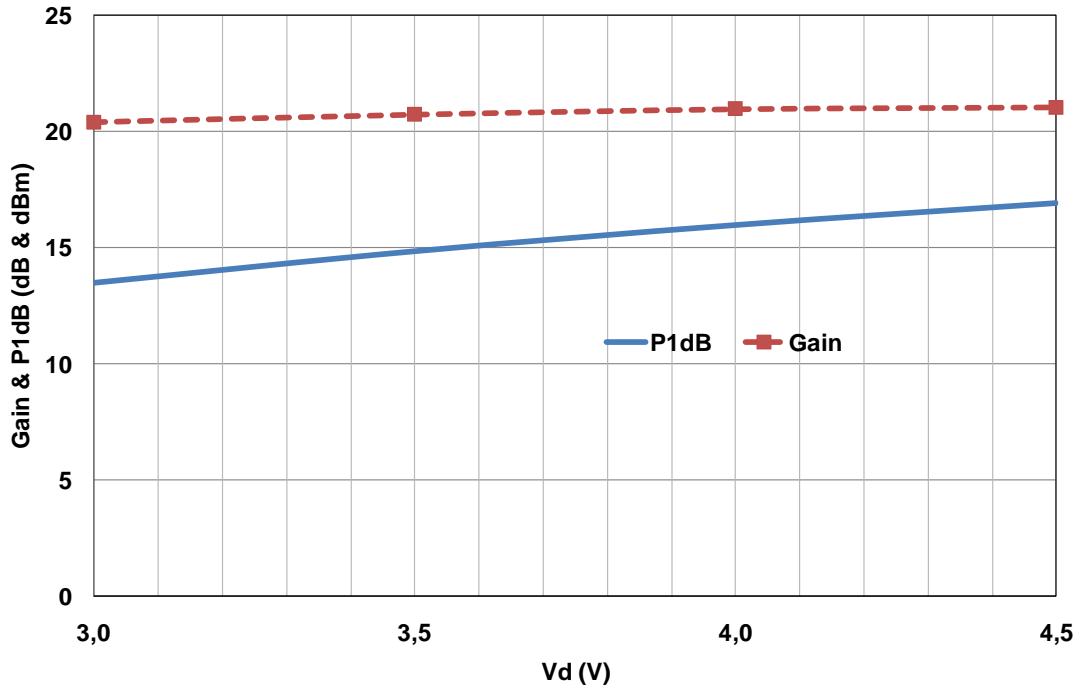
Temp = +25°C, Vd1 = Vd2 = +4.0V, P1 and N2 grounded, P2: NC, typical Id=80mA  
 Measurements in the connector planes, using the proposed land pattern & board 99622.



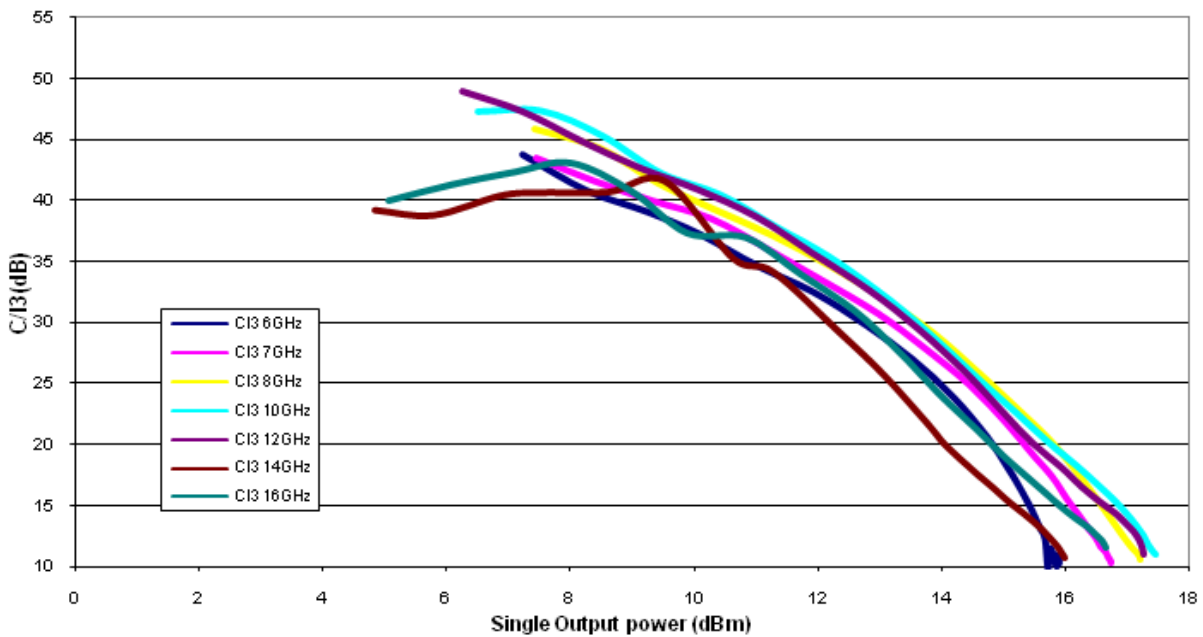
## Typical boards Measurements

Temp = +25°C, Vd1 = Vd2 = +4.0V, P1 and N2 grounded, P2: NC, typical Id=80mA  
 Measurements in the connector planes, using the proposed land pattern & board 99622.

**Output power at 1dB compression and Linear Gain versus Drain Voltage (F=11GHz)**



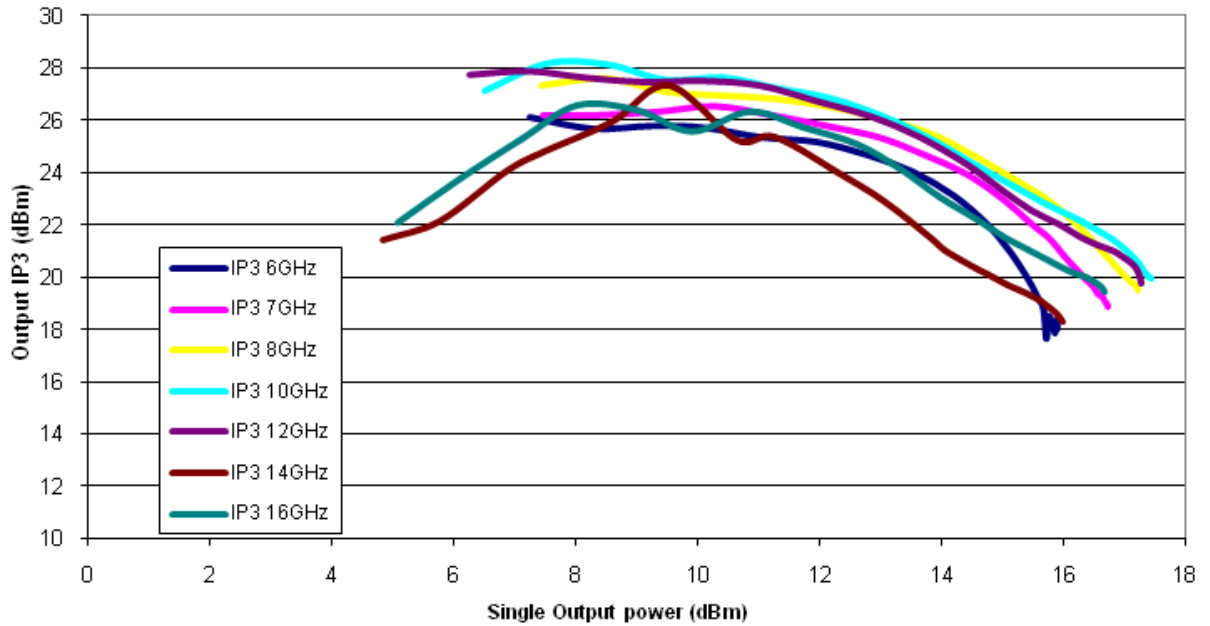
**C/I3 versus output power**



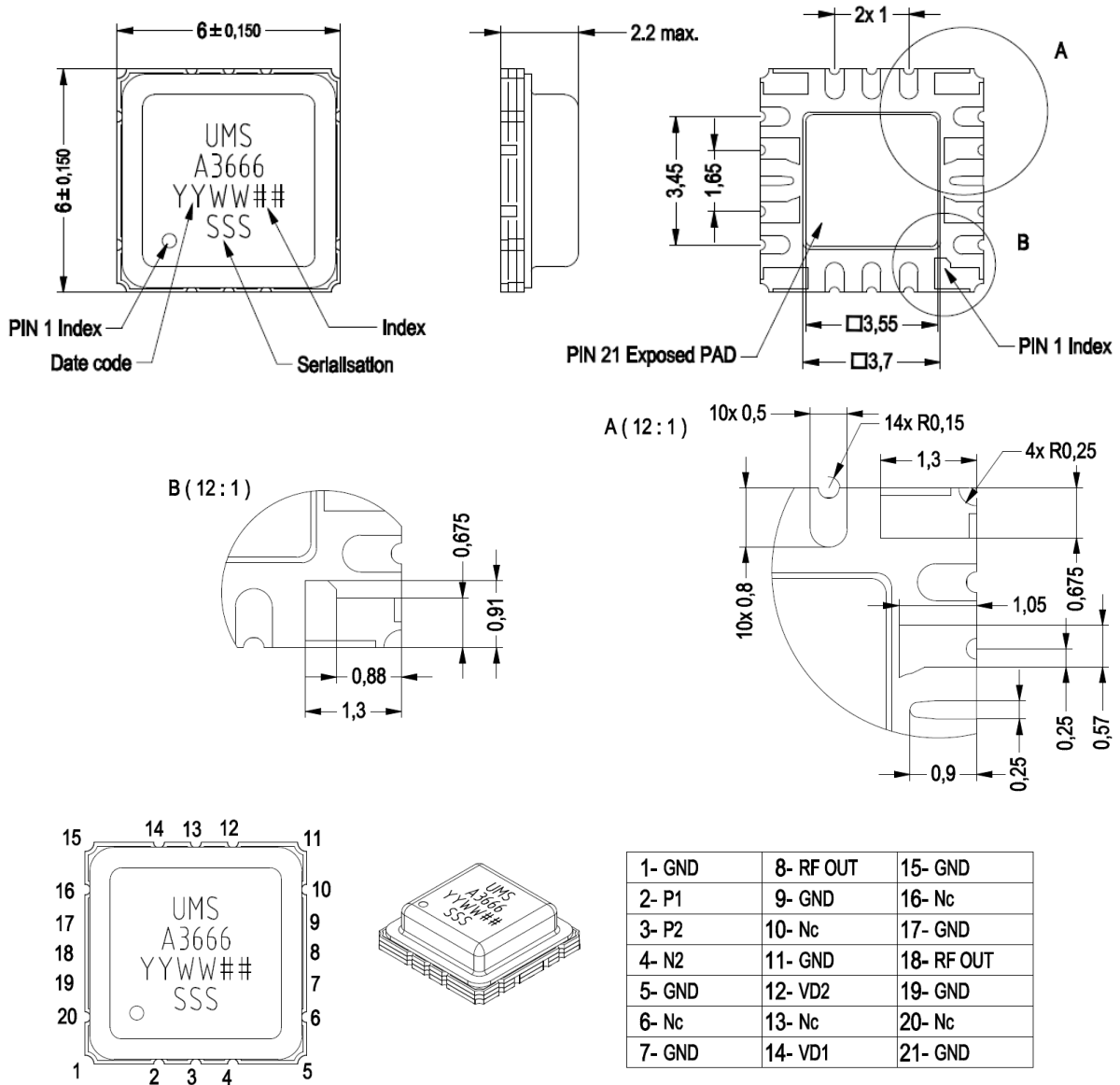
Typical boards Measurements

Temp = +25°C, Vd1 = Vd2 = +4.0V, P1 and N2 grounded, P2: NC, typical Id=80mA  
Measurements in the connector planes, using the proposed land pattern & board 99622.

Output IP3 versus output power



## Package outline (1)



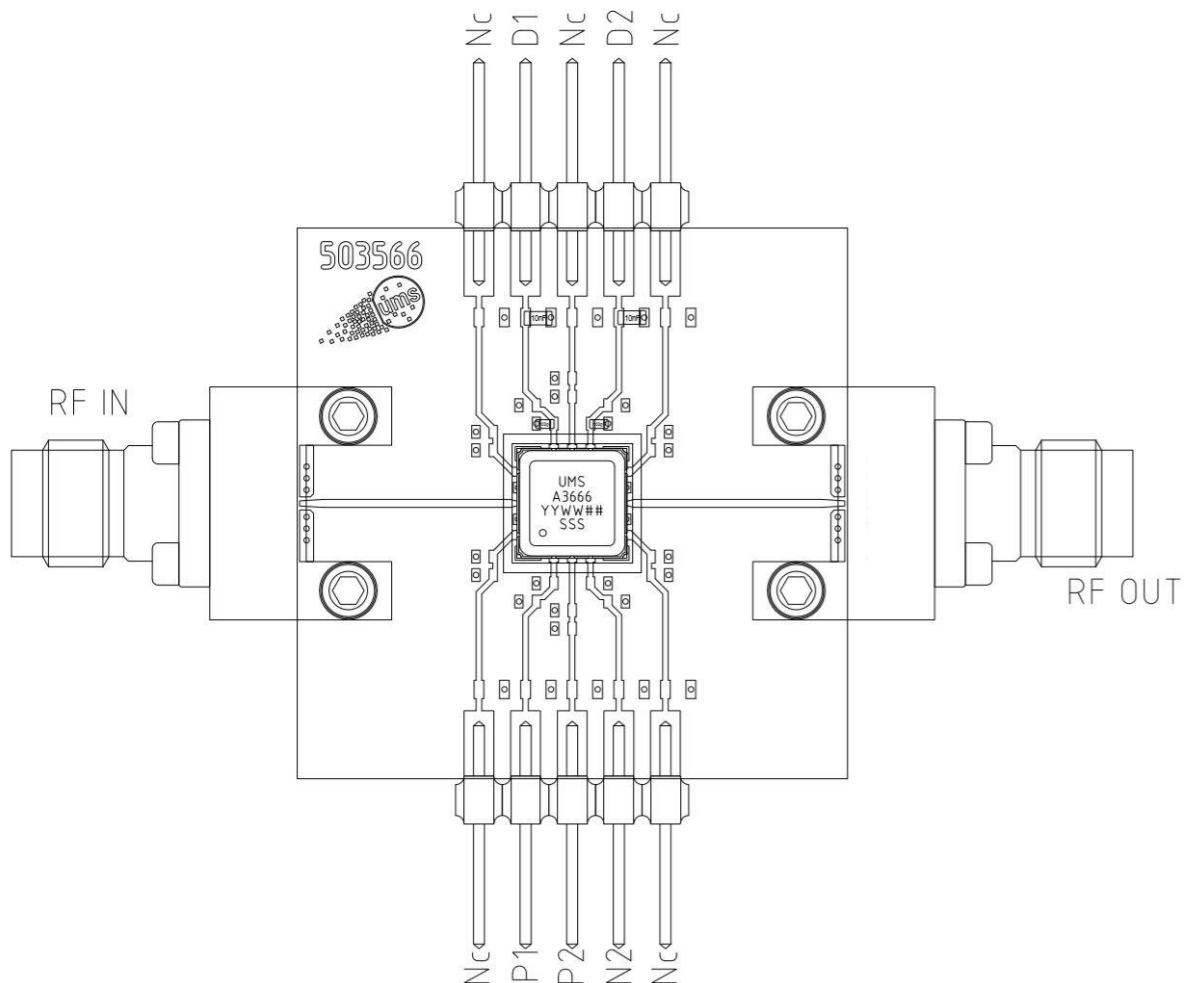
All dimensions are in mm

(1) It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.



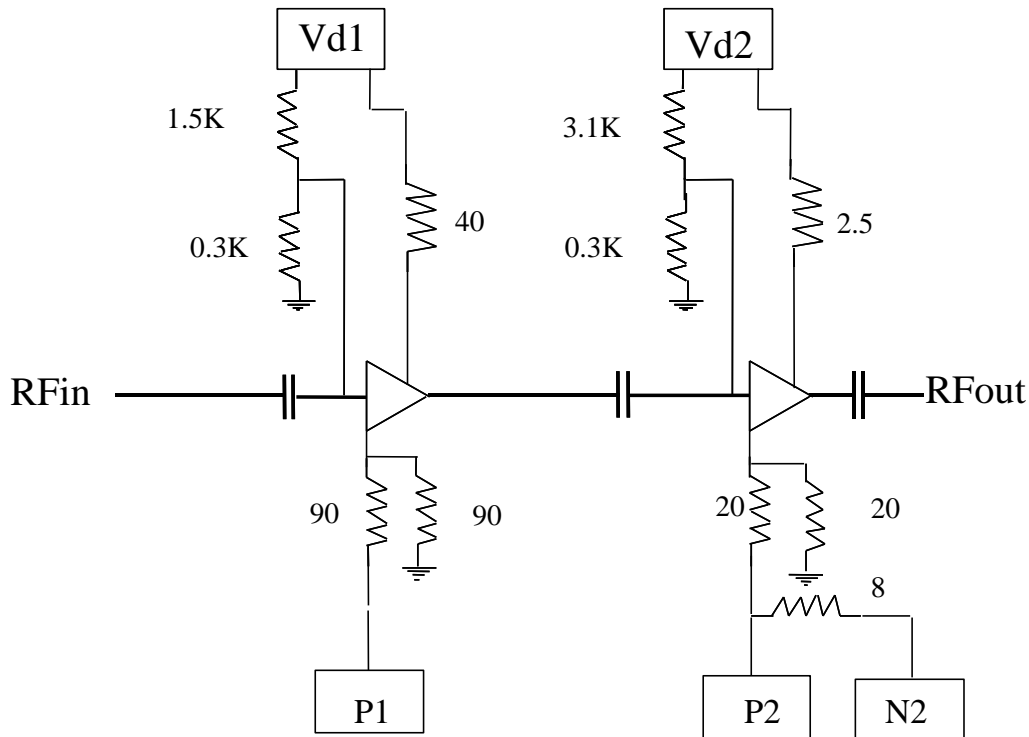
### Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF  $\pm 5\%$  + 10nF  $\pm 10\%$  on D1 and 10nF  $\pm 10\%$  on D2 are recommended for all DC accesses.



## DC Schematic

This chip is self-biased, and flexibility is provided by the access to number of leads. The internal DC electrical schematic is given in order to use these leads in a safe way.



Two standard biasing:

Low Noise and low consumption:

Vd1=Vd2 = 4V and P1, N2 grounded.  
P2 pads non connected (NC).  
Idd = 80mA & Pout-1dB = 16dBm Typical.

Low Noise and higher output power:

Vd1=Vd2 = 4V and P1, P2 grounded.  
N2 pads non connected (NC).  
Idd = 85mA & Pout-1dB = 16.5dBm Typical.

**Note**



## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at <https://www.ums-rf.com>.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

## FAB Type Surface Mount Hermetic Package

Refer to the application note AN0024 available at <https://www.ums-rf.com> for assembly recommendations for the UMS FAB package products.

## Ordering Information

Leadless hermetic package: CHA3666-FAB/XY  
Waffle pack: XY=24

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