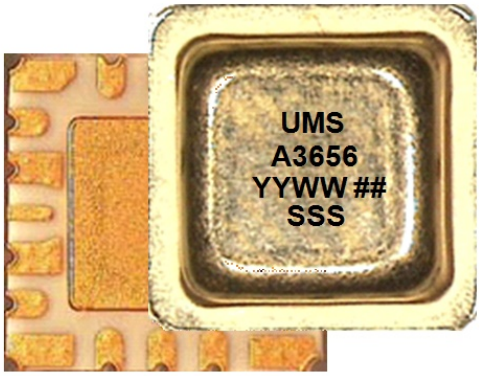
5.8-16GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD Hermetic package

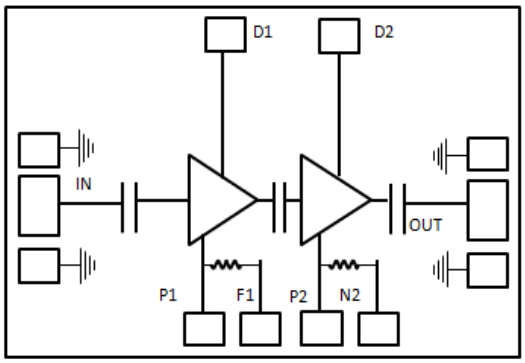
Description

The CHA3656-FAB is a two-stage self-biased wide band monolithic Low Noise Amplifier.
It is dedicated to space communications and also well suited for a wide range of applications, such as C, X, Ku radar, test instrumentation and hi-rel applications.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in a surface mount hermetic package.



Main Features

- Broadband performances: 5.8-16GHz
- 14.5dBm power at 1dB gain compression
- 1.75dB Noise Figure
- 20dB Linear Gain
- DC bias: Vd1=Vd2=3.3V, Id=70mA
- 20 Leads-SMD
- 6x6mm² hermetic metal ceramic package



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.8		16	GHz
Gain	Linear Gain		20		dB
NF	Noise Figure		1.75		dB
Pout	Output Power @1dB comp.		14.5		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics

Tamb.= +25°C, Vd1 = Vd2 = +3.3V, P1 = N2 = GND and F1 = P2 = NC

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.8		16	GHz
Gain	Linear Gain		20		dB
NF	Noise Figure		1.75		dB
IRL	Input Return Loss		8		dB
ORL	Output Return Loss		10		dB
P_{1dB}	Output power for 1dB Gain Compression		14.5		dBm
OIP3	Output 3rd order Intercept Point		25		dBm
Id	Drain bias current		70		mA

These values are representative of on board measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage (Vd1 & Vd2)	4.5	V
Tj	Junction temperature	175	°C
Pin	RF input power	10	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-50 to +150	°C

Typical Bias Conditions

Three biasing options are recommended in paragraph "Recommended Biasing Options".

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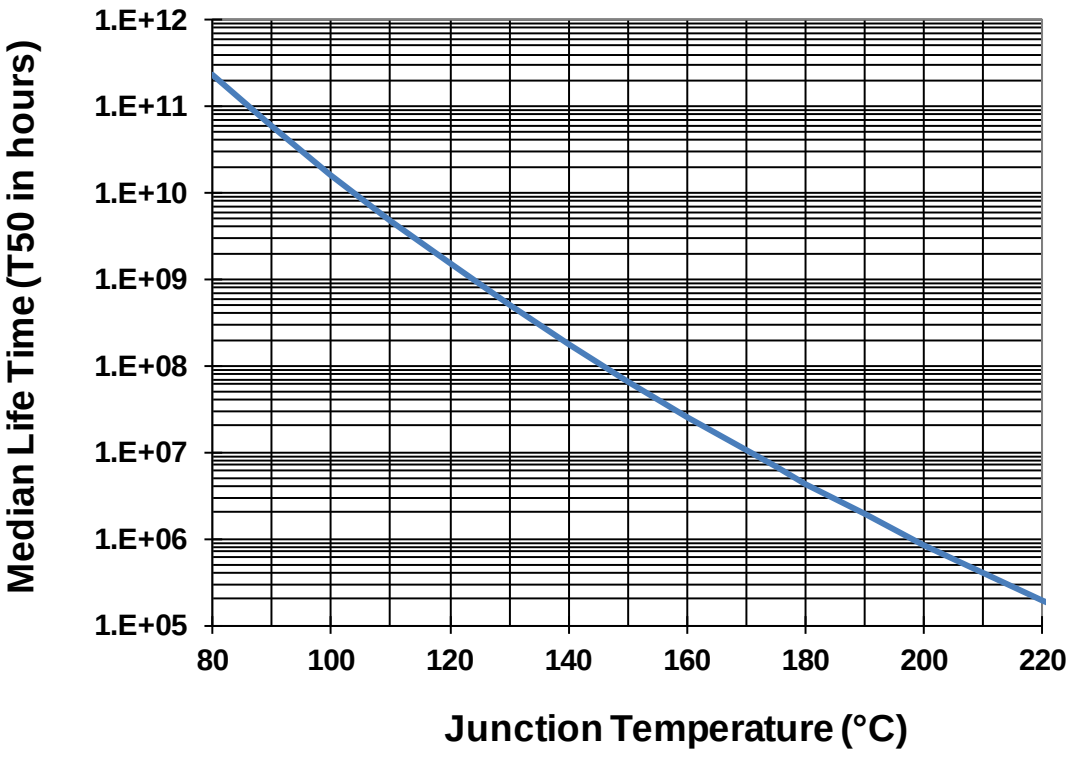
Device thermal performances

All the figures given in this section are obtained assuming that the packaged device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (T_{case}).
The system maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with these requirements.

Parameter	Biasing conditions	$T_{junction}$ (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	F1=P1=N2=P2=NC Vd = 3.3V Idq = 42mA Pdiss = 139mW	111	187	4.5E+09
R_{TH} (1) Thermal Resistance (Junction to Case)	P2=GND Vd = 3.3V Idq = 61mA Pdiss = 202mW	130	223	5.0E+08
R_{TH} (1) Thermal Resistance (Junction to Case)	P1=N2=GND Vd = 3.3V Idq = 65mA Pdiss = 214mW	126	192	8.0E+08

(1) Assuming 85°C T_{case}



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Typical Package Sij parameters

Tamb.= +25°C, Vd1 = Vd2 = 3.3V, Id = 70mA (P1 = N2 = GND and F1 = P2 = NC)

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.00	-0.35	-93.34	-65.61	-176.96	-33.50	-34.35	-0.48	-94.39
3.00	-1.03	-156.89	-61.54	86.29	0.65	-114.06	-3.33	-158.51
4.00	-4.59	94.93	-55.82	-173.48	15.48	112.68	-8.38	165.62
4.50	-7.75	15.63	-48.51	133.25	18.70	49.68	-9.41	150.34
5.00	-8.93	-55.51	-44.70	90.35	20.19	-4.86	-10.06	131.96
5.50	-9.34	-101.36	-42.54	52.24	20.97	-52.25	-10.44	112.05
6.00	-9.84	-129.67	-40.97	19.12	21.40	-94.47	-10.45	90.88
6.50	-10.17	-153.77	-39.78	-11.87	21.61	-133.20	-10.68	71.22
7.00	-10.02	-171.20	-39.07	-40.60	21.70	-169.00	-10.53	46.65
7.50	-9.70	171.24	-38.48	-67.75	21.68	157.41	-10.30	21.71
8.00	-9.53	152.68	-38.15	-93.52	21.64	125.55	-10.10	-3.77
8.50	-9.34	133.93	-37.88	-116.98	21.55	94.88	-10.14	-28.25
9.00	-9.30	113.26	-37.44	-139.94	21.41	65.60	-10.32	-50.52
9.50	-9.50	91.84	-37.03	-163.32	21.33	37.36	-10.61	-70.89
10.00	-9.88	70.17	-36.77	175.19	21.27	9.59	-11.05	-89.31
10.50	-10.28	46.87	-36.39	151.66	21.19	-17.57	-11.46	-104.94
11.00	-10.84	22.12	-36.08	129.60	21.17	-44.45	-11.96	-119.30
11.50	-11.48	-3.99	-35.83	107.34	21.15	-71.55	-12.45	-132.85
12.00	-12.16	-30.33	-35.65	85.13	21.10	-98.50	-12.92	-144.83
12.50	-12.66	-56.67	-35.55	63.71	20.98	-125.45	-13.40	-155.39
13.00	-12.86	-81.68	-35.50	41.81	20.79	-152.48	-13.83	-167.14
13.50	-12.83	-104.28	-35.53	21.79	20.49	-178.75	-14.56	-178.85
14.00	-11.83	-124.90	-35.68	-2.20	20.26	157.09	-16.21	177.62
14.50	-10.93	-143.78	-36.05	-19.00	20.25	131.24	-16.74	168.00
15.00	-9.49	-163.97	-36.07	-39.29	20.26	104.99	-17.71	168.37
15.50	-8.32	175.72	-36.78	-59.00	20.12	77.76	-18.25	166.78
16.00	-7.08	154.86	-37.09	-78.28	19.92	50.34	-17.95	169.76
16.50	-5.86	133.85	-37.18	-94.54	19.69	22.92	-16.74	173.82
17.00	-5.14	110.72	-37.77	-117.70	19.26	-5.44	-15.17	166.62
17.50	-4.86	88.04	-39.38	-138.25	18.58	-33.25	-13.82	155.04
18.00	-4.83	65.44	-40.35	-147.24	17.80	-59.97	-12.89	139.09
18.50	-5.14	44.70	-41.17	-164.04	17.07	-85.50	-12.71	122.55
19.00	-5.51	22.33	-41.31	-173.91	16.45	-111.50	-12.64	105.92
19.50	-6.28	-0.76	-41.57	171.01	15.70	-137.82	-12.65	85.59
20.00	-7.50	-25.25	-40.69	160.07	14.90	-164.10	-13.13	62.35
21.00	-10.97	-84.33	-38.82	113.26	12.98	143.71	-13.17	2.24
22.00	-13.83	-174.86	-37.72	68.16	10.73	91.97	-11.26	-67.68
23.00	-10.64	103.63	-37.04	14.78	7.81	42.57	-8.39	-121.25
24.00	-7.55	52.15	-36.67	-37.79	4.56	-1.91	-6.02	-161.58
25.00	-5.85	13.50	-37.86	-79.55	1.42	-41.12	-4.54	167.08

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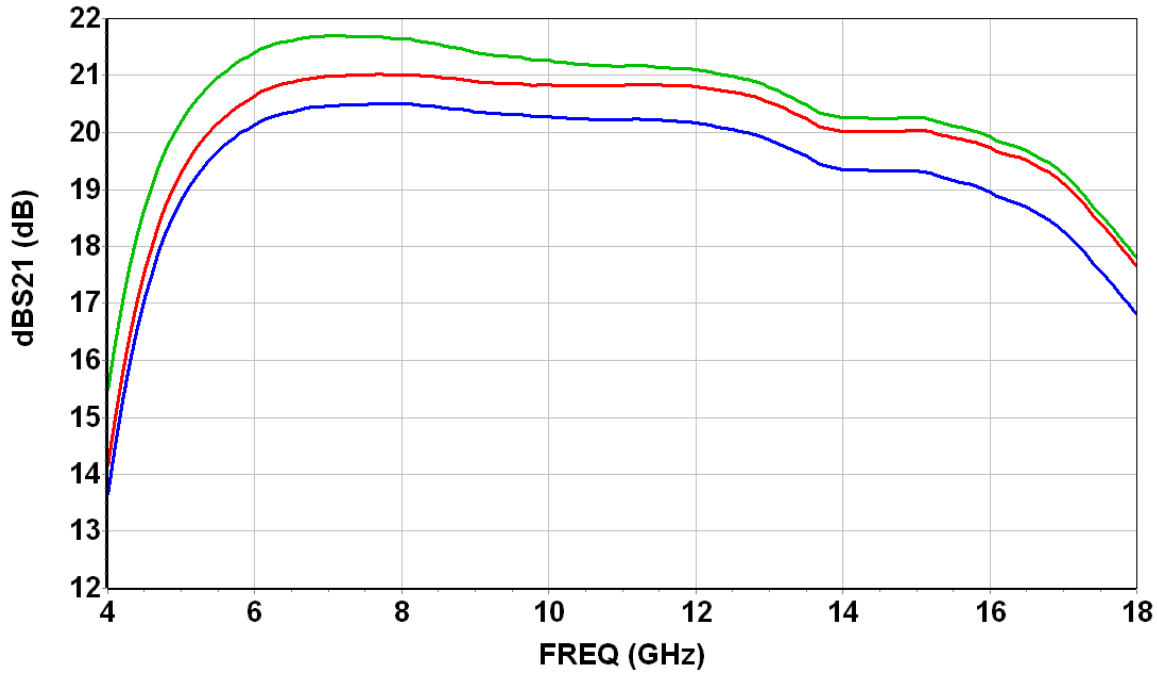
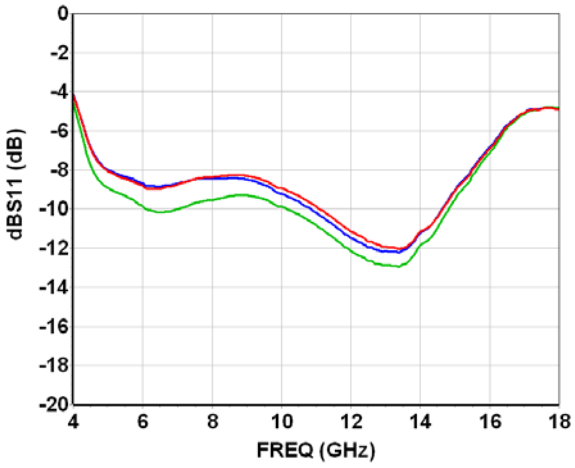
Typical Package Measurements

Tamb.= +25°C, Vd1 = Vd2 = 3.3V, 3 biasing options to get :
Id = 70mA (P1 = N2 = GND and F1 = P2 = Not connected)
Id = 64mA (P2 = GND and F1 = P1 = P2 = Not connected)
Id = 47mA (F1 = P1 = N2 = P2 = Not connected)

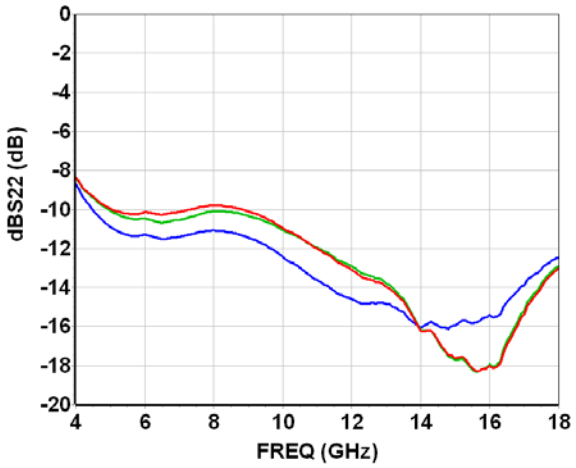
Linear Gain versus Frequency and Id



Input Return Loss vs. Frequency and Id



Output Return Loss vs. Frequency and Id



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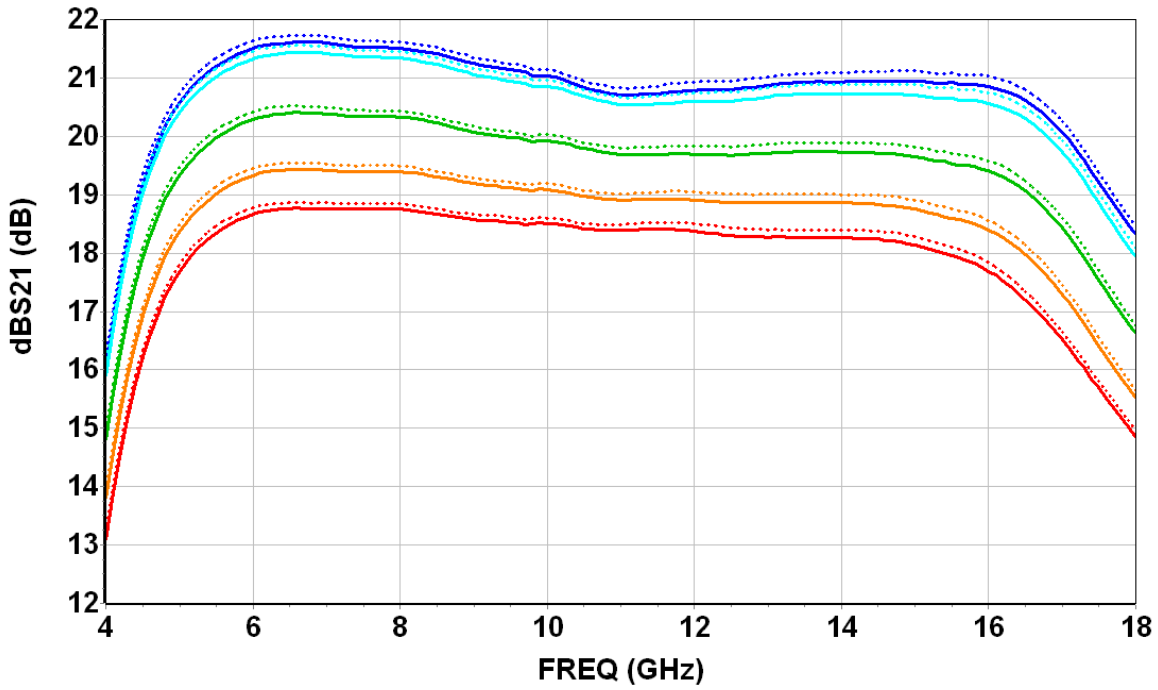
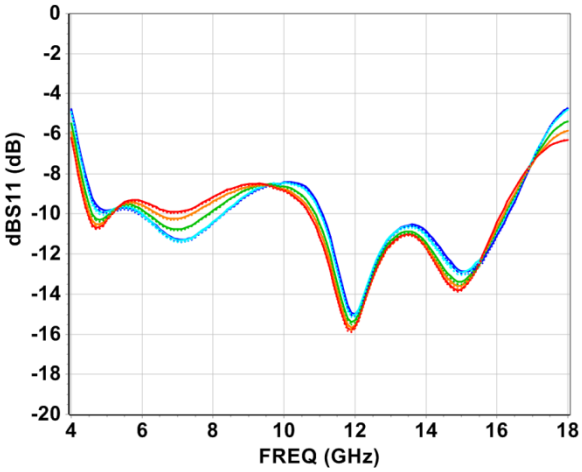
Typical Board Measurements

Temperature : -50, -40, +25, +85, +125°C
Vd1 = Vd2 = 3.3V (dot lines) and 3V (solid lines)
Id = 70mA (P1 = N2 = GND and F1 = P2 = Not connected)

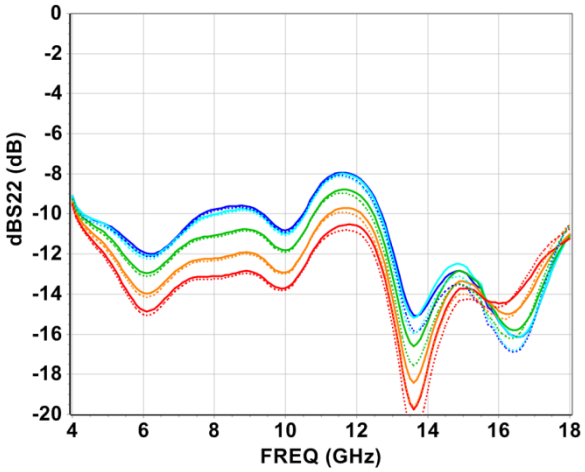
Linear Gain versus Frequency, Temperature and Vd



Input Return Loss vs. Frequency, Temperature and Vd



Output Return Loss vs. Frequency, Temperature and Vd



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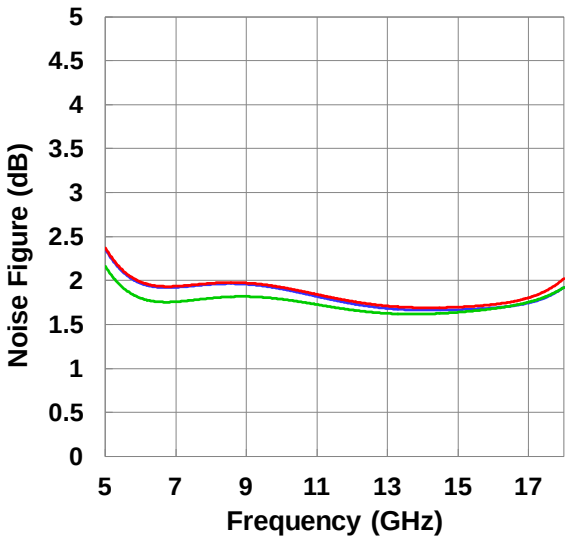
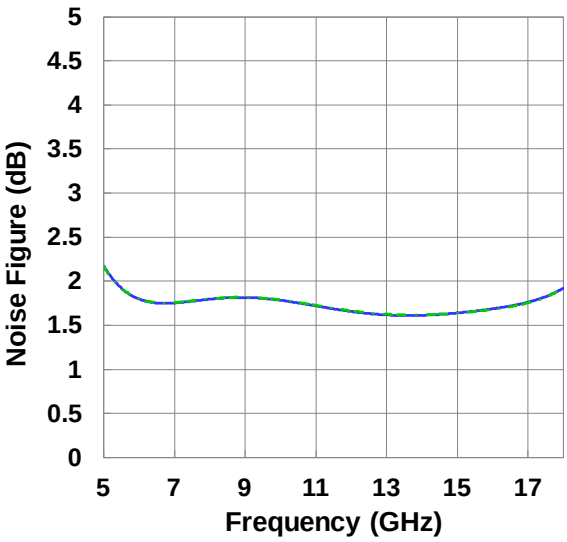
Typical Board Measurements

Tamb.= +25°C, Vd = Vd1 = Vd2
Id = 70mA (P1 = N2 = GND and F1 = P2 = Not connected)

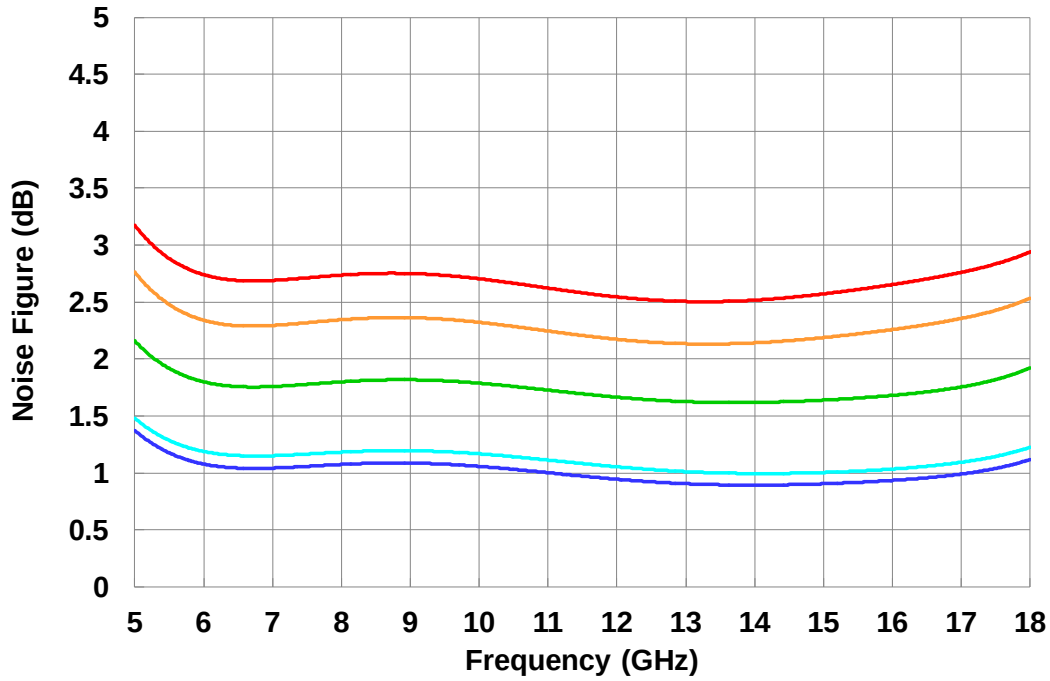
Noise Figure vs. Frequency and Id
Vd = 3.3V; Id = 47mA, 64mA, 70mA



Noise Figure vs. Frequency and Vd
Vd = 3V, 3.3V; Id = 70mA



Noise Figure versus Frequency and Temperature
Vd = 3.3V; Id = 70mA
Temperature : -50, -40, +25, +85, +125°C



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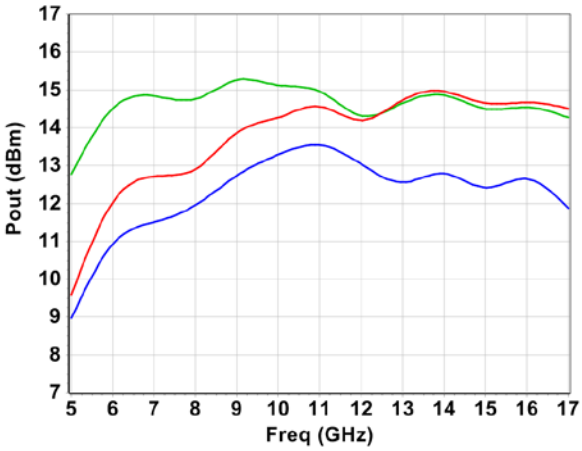
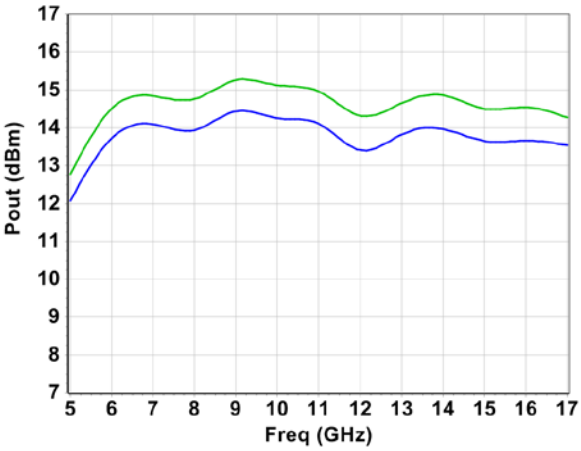
Typical Board Measurements

Tamb.= +25°C, Vd = Vd1 = Vd2
Id = 70mA (P1 = N2 = GND and F1 = P2 = Not connected)

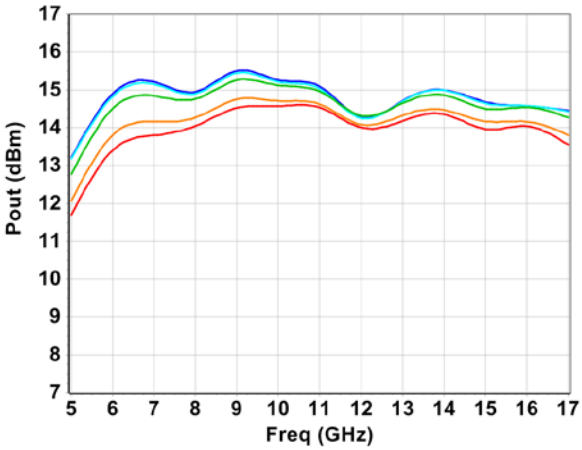
P_{1dB} versus Frequency and Id
Vd = 3.3V; Id = 47mA, 64mA, 70mA



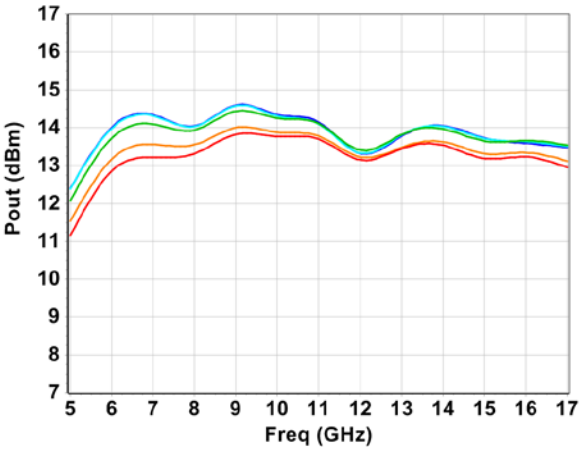
P_{1dB} versus Frequency and Vd
Vd = 3V, 3.3V; Id = 70mA



P_{1dB} vs. Frequency and Temperature
Vd = 3.3V; Id = 70mA
Temp : -50, -40, +25, +85, +125°C



P_{1dB} vs. Frequency and Temperature
Vd = 3V; Id = 70mA
Temp : -50, -40, +25, +85, +125°C



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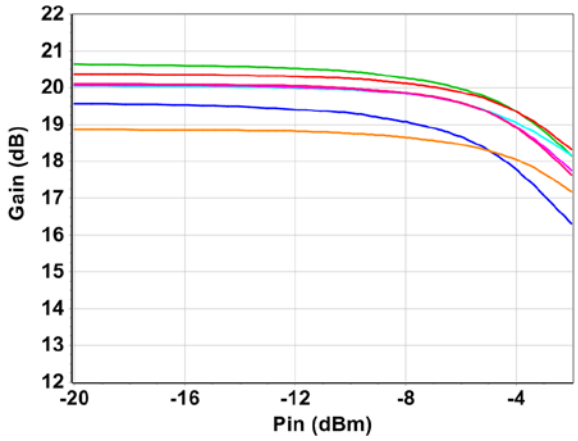
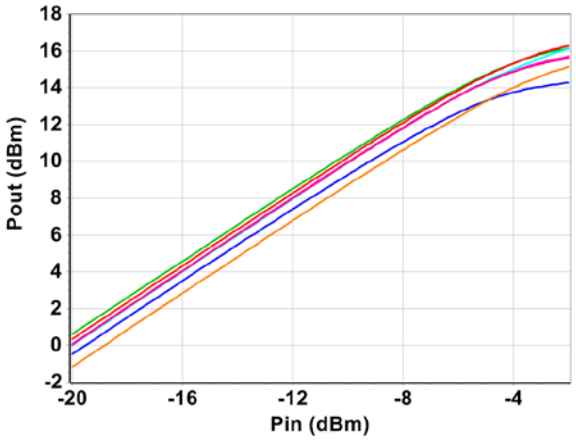
Typical Board Measurements

Tamb.= +25°C, Vd1 = Vd2 = 3.3V
Id = 70mA (P1 = N2 = GND and F1 = P2 = Not connected)

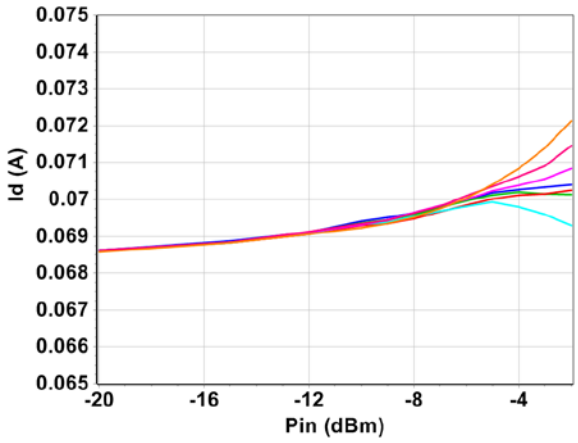
Gain versus Pin and Frequency
Freq : 5, 7, 9, 11, 13, 15, 17GHz



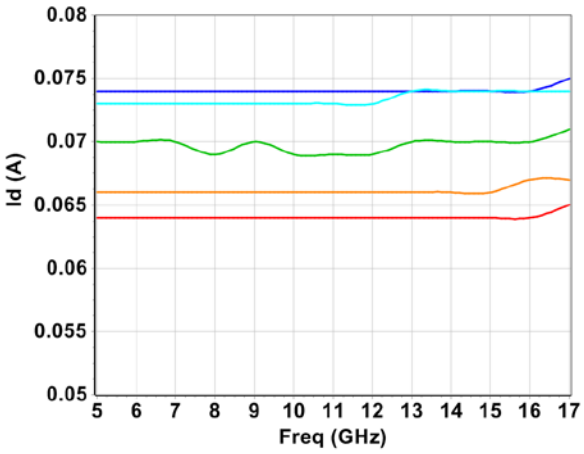
Pout versus Pin and Frequency
Freq : 5, 7, 9, 11, 13, 15, 17GHz



Id versus Pin and Frequency
Freq : 5, 7, 9, 11, 13, 15, 17GHz



Id at P1dB vs Frequency and Temperature
Freq : 5, 7, 9, 11, 13, 15, 17GHz



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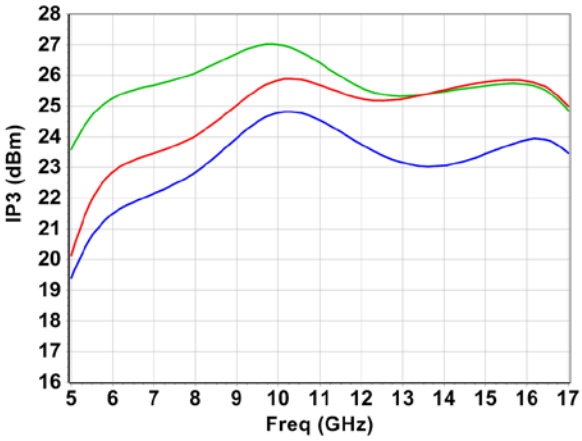
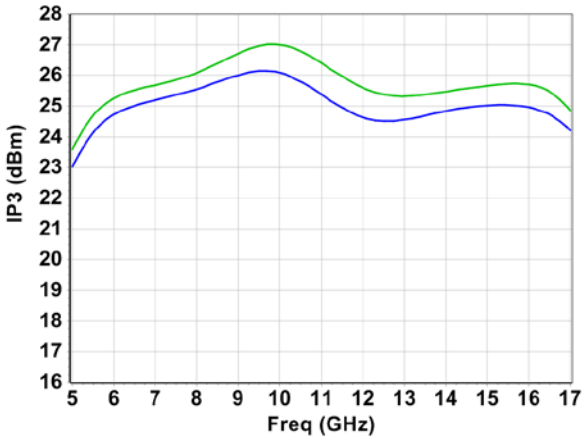
Typical Board Measurements

Tamb.= +25°C, Vd = Vd1 = Vd2
Id = 70mA (P1 = N2 = GND and F1 = P2 = Not connected)

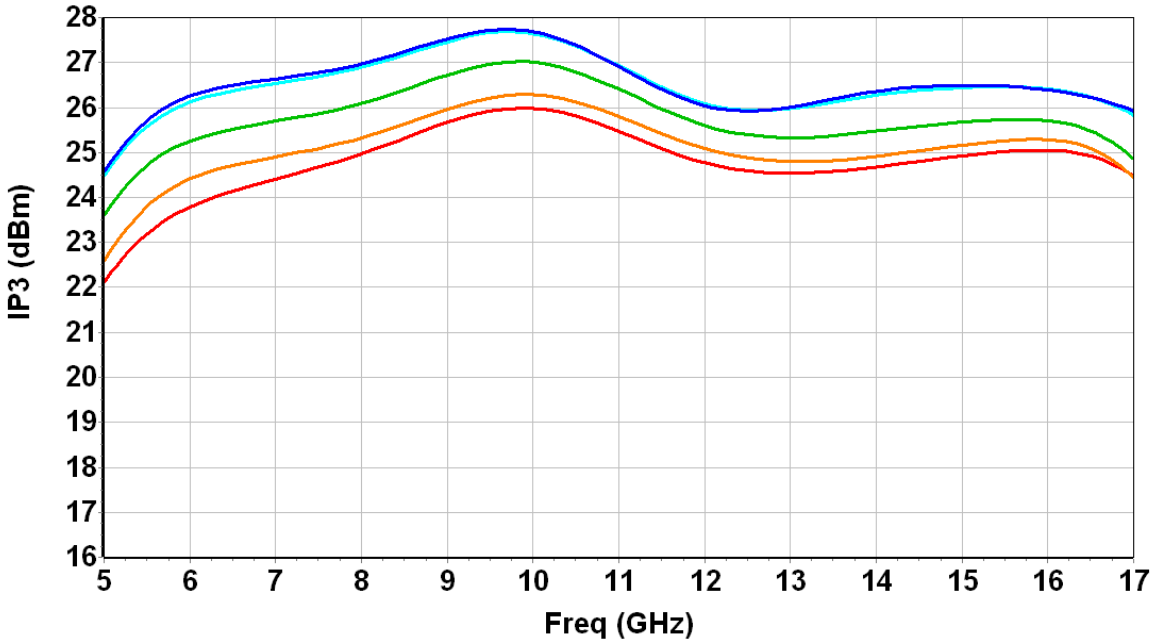
Output IP3 versus Frequency and Id
Vd = 3.3V; Id = 47, 64, 70mA



Output IP3 versus Frequency and Vd
Vd = 3V, 3.3V; Id = 70mA



Output IP3 versus Frequency and Temperature
Vd = 3.3V; Id = 70mA
Temperature : -50, -40, +25, +85, +125°C



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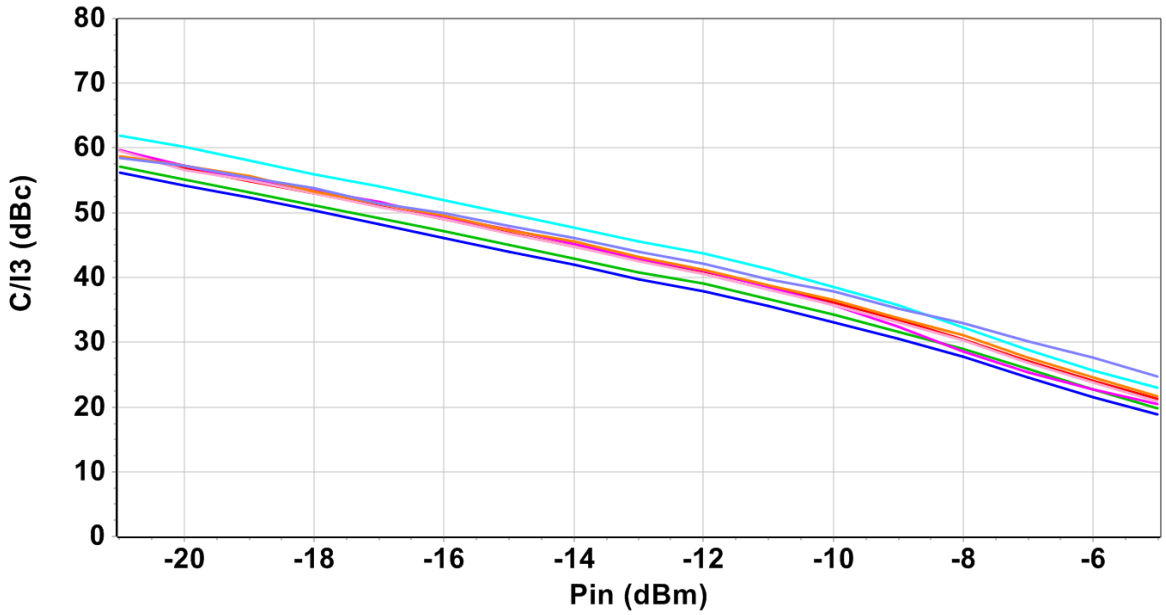
Typical Board Measurements

Tamb.= +25°C, Vd1 = Vd2 = 3.3V
Id = 70mA (P1 = N2 = GND and F1 = P2 = Not connected)

C/I3 versus Pin and Frequency
Freq : 5, 6, 8, 10, 12, 14, 16, 17GHz



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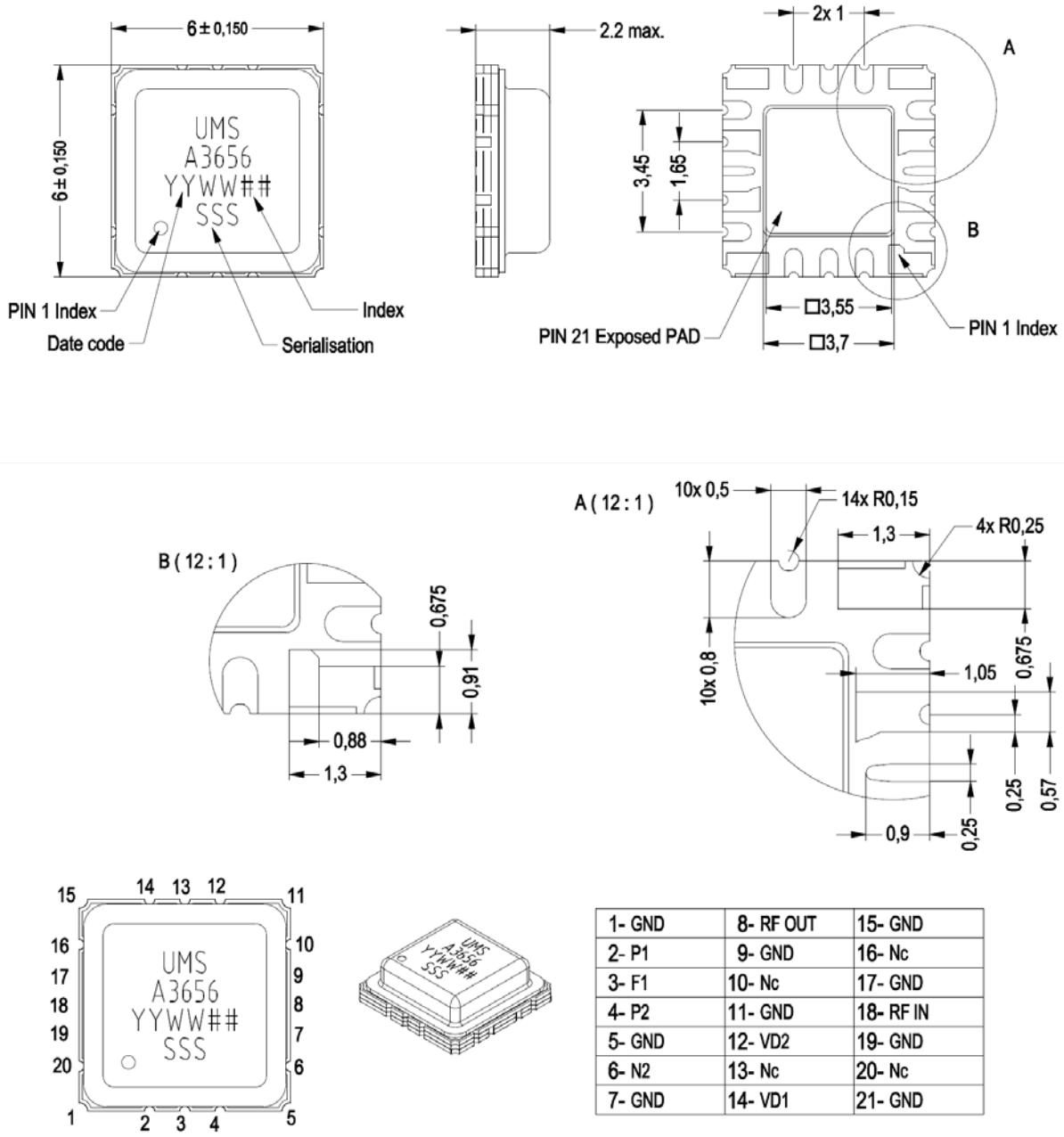
Package outline (1)



1- GND	8- RF OUT	15- GND
2- P1	9- GND	16- Nc
3- F1	10- Nc	17- GND
4- P2	11- GND	18- RF IN
5- GND	12- VD2	19- GND
6- N2	13- Nc	20- Nc
7- GND	14- VD1	21- GND

All dimensions are in mm

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0024 (https://www.ums-rf.com) for exact package dimensions.

It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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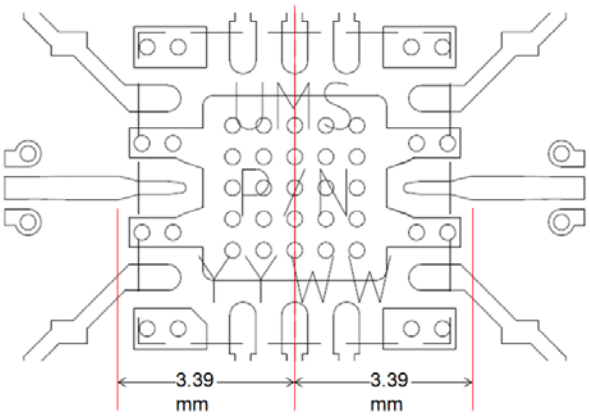
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.39mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Package Information

Parameter	Value
Package body material	RoHS-compliant
Lead finish	Gold
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	$1x10^{-8}$ccHe/s/atm

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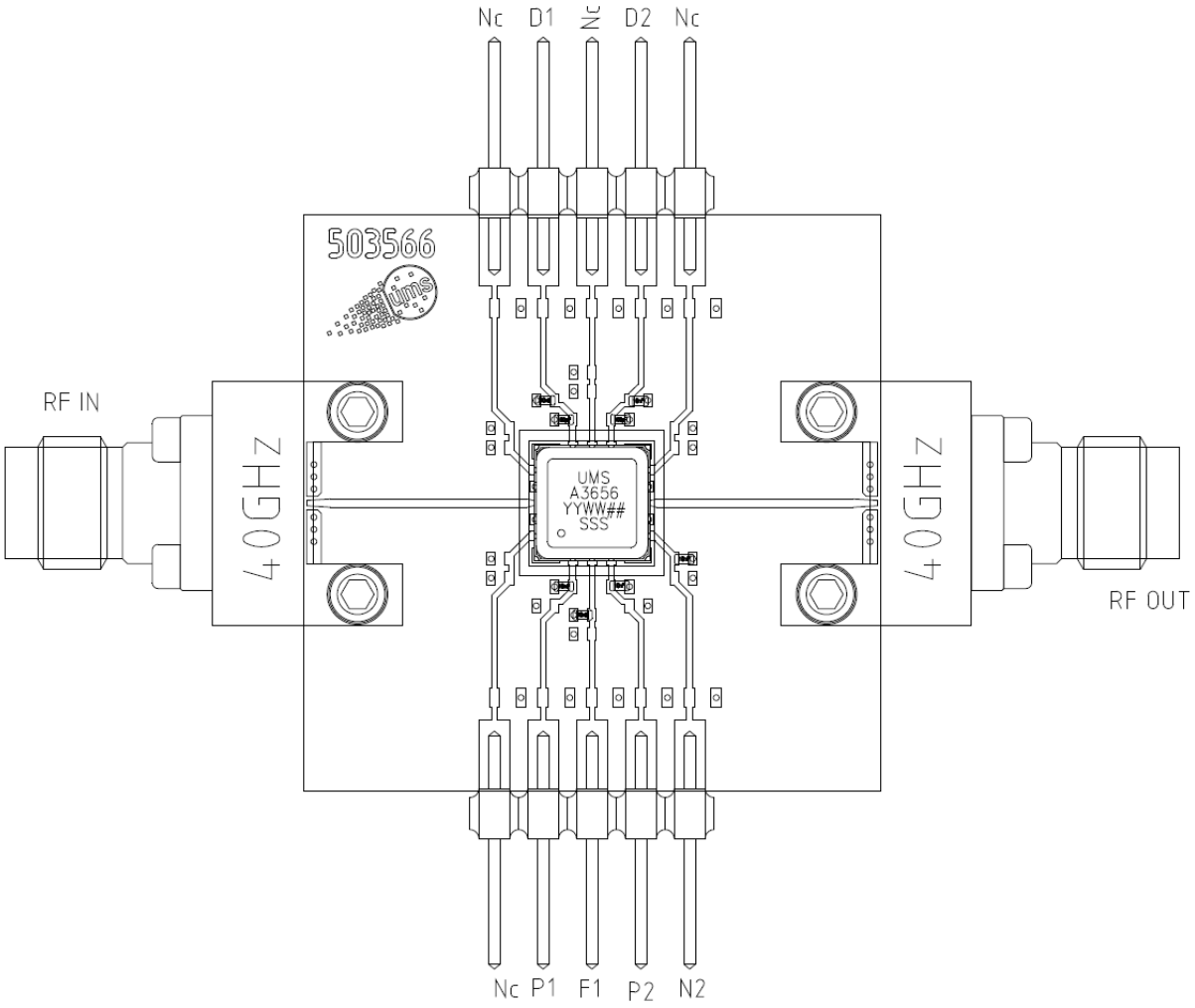
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5% & 10nF ±10% are recommended for all DC accesses.
- See application note AN0024 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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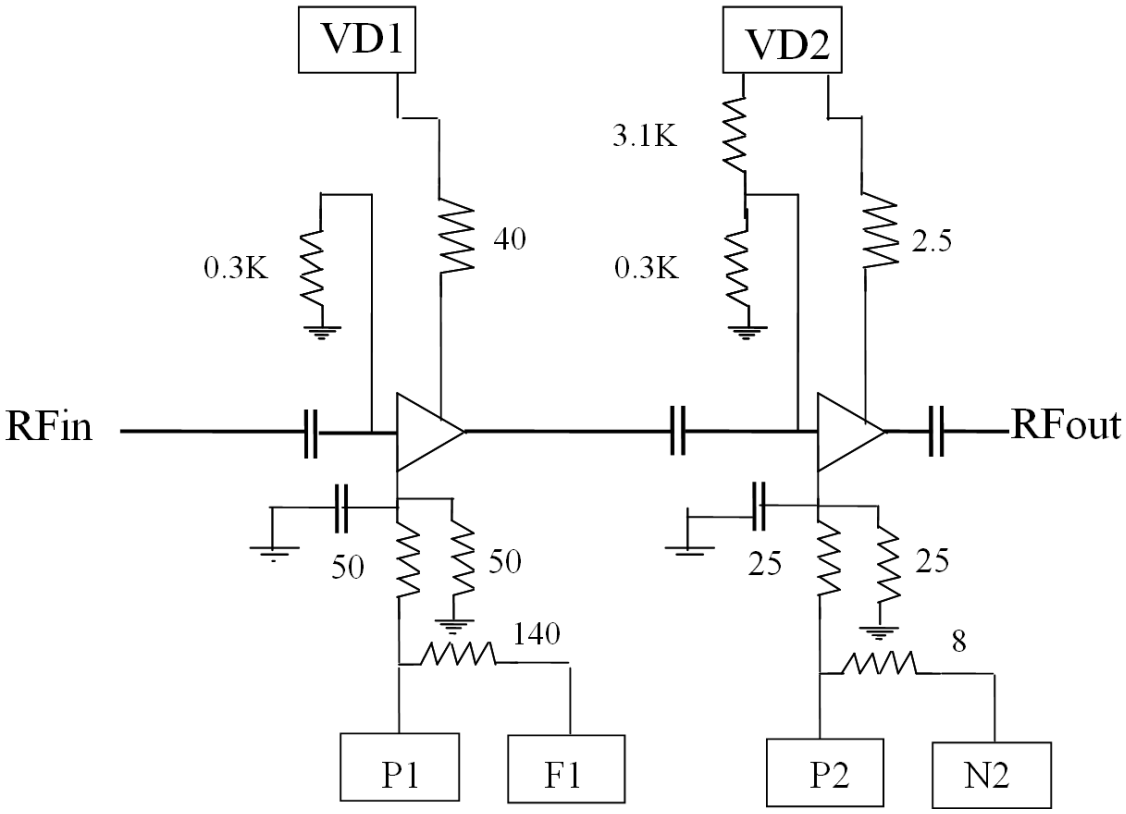
DC Schematic



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Recommended Biasing Options

Biasing option 1	Standard biasing
	Vd1 = Vd2 = 3.3V and Id = 70mA P1 = N2 = GND and F1 = P2 = Not connected At Tamb. = +25°C : Typ. Gain = 20dB / Typ. P1dB = 14.5dBm / Typ. OIP3 = 25dBm

Biasing option 2	Compromise Id & P1dB
	Vd1 = Vd2 = 3.3V and Id = 64mA P2 = GND and F1 = P1 = P2 = Not connected At Tamb. = +25°C : Typ. Gain = 19.5dB / Typ. P1dB = 14dBm / Typ. OIP3 = 24.5dBm

Biasing option 3	Reduced current (Id)
	Vd1 = Vd2 = 3.3 V and Id = 47mA F1 = P1 = N2 = P2 = Not connected At Tamb. = +25°C : Typ. Gain = 19dB / Typ. P1dB = 12.5dBm / Typ. OIP3 = 23dBm

It is possible to bias Vd1 = Vd2 = 3V on these biasing options, with (as compared to 3.3V):

ΔId	-2	mA
ΔGain	-0.2	dB
ΔP1dB	-0.7	dB
ΔOIP3	-0.7	dB
ΔTj	-2	°C

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Notes

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Recommended package footprint for FAB Package

Refer to the application note AN0024 available at https://www.ums-rf.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure for FAB Package

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details see application note AN0024 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Leadless hermetic package:	CHA3656-FAB/XY Waffle pack: XY=24

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