

27-33.5GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

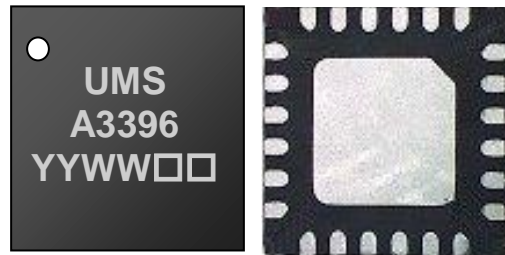
Description

The CHA3396-QDG is a 3 stage monolithic Medium Power Amplifier, which produces 22dB gain for 19dBm output power.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

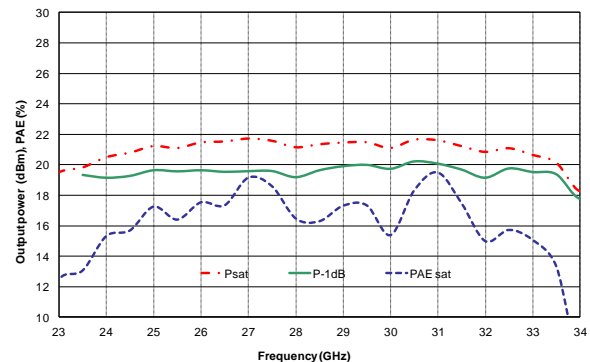
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 27-33.5GHz
- 19dBm Pout at 1dB compression
- 22dB gain
- 30dBm OTOI
- DC bias: Vd= 4.0V, Id= 155mA
- 24L-QFN4x4 (QDG)
- MSL1

Output Power & PAE versus Frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.0		33.5	GHz
Gain	Linear Gain		22		dB
P-1dB	Output Power @1dB comp.		19		dBm
OTOI	3 rd order Intercept point		30		dBm

Electrical Characteristics

T_{amb.} = +25°C, V_d = +4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27		33.5	GHz
Gain	Linear Gain		22		dB
ΔG	Gain variation in temperature		0.026		dB/°C
G _{CTRL}	Gain control range		15		dB
OTOI	3 rd order Intercept point		30		dBm
P _{-1dB}	Output power @ 1dB compression		19		dBm
Psat	Saturated Output Power		21		dBm
RLin	Input Return Loss		10		dB
RLout	Output Return Loss		13		dB
NF	Noise figure		4.5		dB
I _d	Quiescent Drain current		155		mA
V _g	Gate voltage		-0.35		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

“Power ON” sequence

1. Ground the device
2. Bias MPA gate voltage at V_g low enough (Typically: V_g ≈ -1V)
3. Apply V_{ds} bias voltage (Typically: V_d = 4V)
4. Increase slowly V_{gs} up to quiescent bias drain current I_{dq}
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias MPA gate voltage at V_g low enough (Typically: V_g ≈ -1V)
3. Turn V_{ds} bias voltage to 0V
4. Turn V_{gs} bias voltage to 0V

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	4.5V	V
I _d	Drain bias quiescent current	200	mA
V _g	Gate bias voltage	-2 to +0.4	V
V _{dg}	External drain-gate excursion	5	V
P _{in}	Maximum input power	6	dBm
T _j	Maximum junction temperature ⁽²⁾	175	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Thermal Resistance channel to ground paddle

⁽²⁾ Thermal Resistance channel to ground paddle = 100.9°C/W for T_{amb.} = +85°C with 4.0V & 155mA.

Recommended Operating Range ^{3, 4}

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	3.3 to 4	V
I _d	Drain bias current	100 to 155	mA
V _g	Gate bias voltage	-1 to 0	V
P _{in}	Maximum peak input power overdrive	5	dBm

⁽³⁾ Electrical performances are defined for specified test conditions

⁽⁴⁾ Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

T _a	Operating temperature range	-40 to +95	°C
T _{stg}	Storage temperature range	-55 to +150	°C

Typical Bias ConditionsT_{amb.} = +25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1	8	DC Gate voltage 1 st stage	-0.35	V
VG2	9	DC Gate voltage 2 nd stage	-0.35	V
VG3	10	DC Gate voltage 3 rd stage	-0.35	V
VD1	23	DC Drain voltage 1 st stage	4.0	V
VD2	22	DC Drain voltage 2 nd stage	4.0	V
VD3	21	DC Drain voltage 3 rd stage	4.0	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).

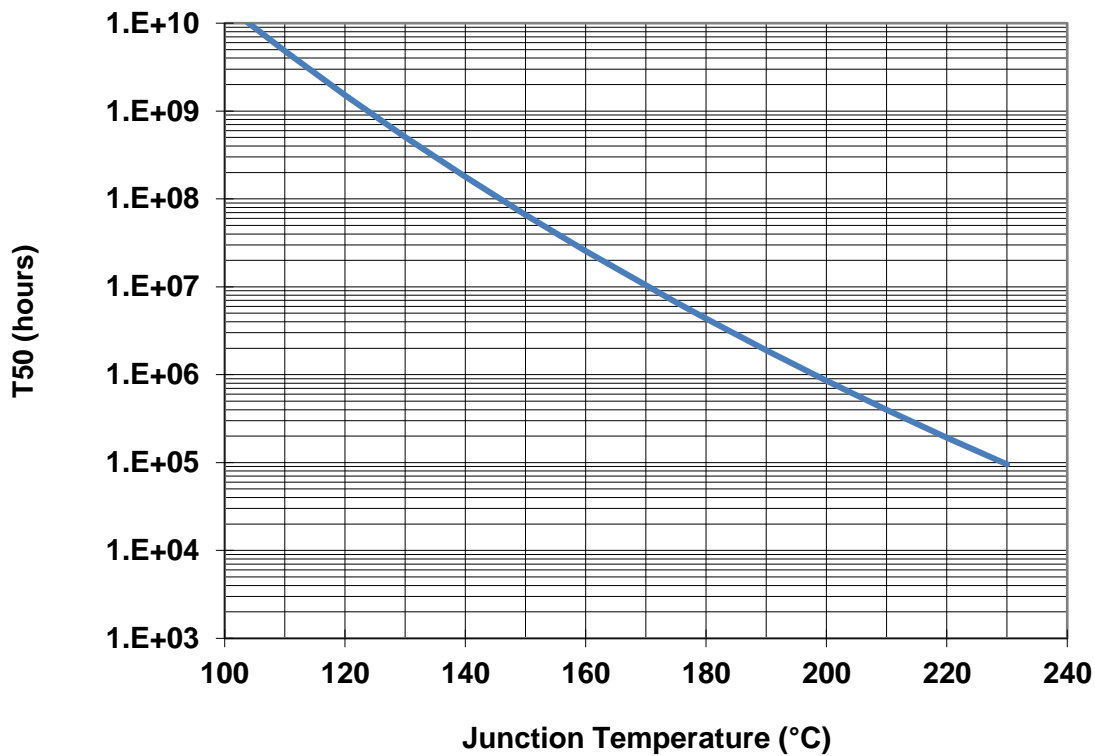
The temperature is monitored at the package back-side interface (Tcase).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH ⁽¹⁾ Thermal Resistance (Junction to Case)	Vd= 4V Id= 155mA Pdiss= 0.62W	156	114.5	3.71E+07

¹ Assuming 85°C Tcase



Typical Package Sij parameters

Tamb.= +25°C, Vd = +4V, Id = 155mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
2	-0.177	135.6	-67.577	20.7	-67.178	34.5	-0.962	108.6
3	-0.249	113.5	-66.628	11.6	-64.533	-2.4	-1.094	71.9
4	-0.306	90.9	-66.419	20.1	-66.730	-15.2	-1.267	34.2
5	-0.374	68.4	-61.518	10.3	-71.920	-38.2	-1.453	-3.4
6	-0.478	45.9	-53.854	-31.1	-71.094	92.0	-1.688	-42.0
7	-0.614	23.3	-43.534	-85.5	-61.481	58.6	-2.020	-81.2
8	-0.711	1.4	-33.949	-170.4	-58.074	22.8	-2.652	-121.3
9	-0.908	-20.5	-26.532	116.7	-52.430	-24.8	-3.367	-163.5
10	-1.008	-41.9	-20.149	47.3	-52.007	-78.0	-4.663	152.3
11	-1.109	-63.1	-14.839	-21.7	-51.030	-140.2	-6.852	106.2
12	-1.111	-84.1	-12.112	-91.4	-52.842	168.9	-8.188	72.4
13	-1.118	-105.5	-9.836	-145.6	-54.224	119.1	-8.950	28.3
14	-1.110	-127.4	-7.538	167.5	-52.192	131.3	-9.428	-14.8
15	-1.178	-150.8	-5.046	120.8	-48.327	77.1	-10.532	-55.3
16	-1.228	-173.9	-2.488	76.5	-49.967	44.3	-12.115	-93.0
17	-1.284	161.5	0.190	32.5	-46.997	18.8	-14.194	-129.4
18	-1.367	136.7	2.997	-11.0	-48.992	-2.1	-16.885	-168.3
19	-1.541	109.7	5.939	-55.7	-48.651	-16.3	-21.242	151.8
20	-1.765	81.9	8.897	-101.6	-51.248	-22.7	-28.518	111.7
21	-2.027	53.3	11.893	-149.9	-50.772	-26.7	-35.954	-109.2
22	-2.409	23.3	14.859	159.2	-52.372	-30.4	-22.292	-152.1
23	-3.099	-7.9	17.571	104.6	-50.227	-21.7	-16.442	157.5
24	-4.313	-39.8	19.646	47.8	-48.337	-23.6	-13.242	114.4
25	-5.869	-72.3	21.219	-10.3	-48.669	-33.3	-11.683	72.7
26	-8.557	-109.6	22.154	-68.0	-44.901	-39.4	-11.452	36.9
27	-12.434	-139.6	22.757	-123.6	-43.561	-33.3	-12.756	1.8
28	-16.855	-179.1	23.288	179.6	-38.962	-51.3	-14.025	-32.4
29	-25.143	157.1	23.436	123.5	-37.464	-88.5	-16.954	-82.6
30	-43.068	141.2	23.316	65.7	-35.734	-110.1	-21.978	-167.0
31	-23.546	-101.3	22.507	9.3	-35.719	-128.1	-24.820	159.2
32	-17.647	-132.3	21.717	-45.1	-34.429	-155.4	-28.188	129.0
33	-11.284	-161.2	21.245	-95.9	-35.382	162.9	-18.619	-180.0
34	-8.198	167.9	20.909	-156.4	-37.963	138.1	-12.747	146.1
35	-5.091	141.7	19.425	139.1	-42.719	109.8	-8.483	122.3
36	-3.086	111.1	16.200	75.2	-55.617	106.5	-5.934	87.2
37	-1.780	83.2	12.163	20.9	-49.723	-158.7	-4.789	57.0
38	-1.272	59.2	8.109	-26.9	-42.745	-171.0	-4.701	27.7
39	-0.999	38.2	4.609	-71.0	-39.377	170.3	-5.397	-2.6
40	-0.868	19.8	1.638	-116.5	-36.317	138.4	-8.063	-37.6

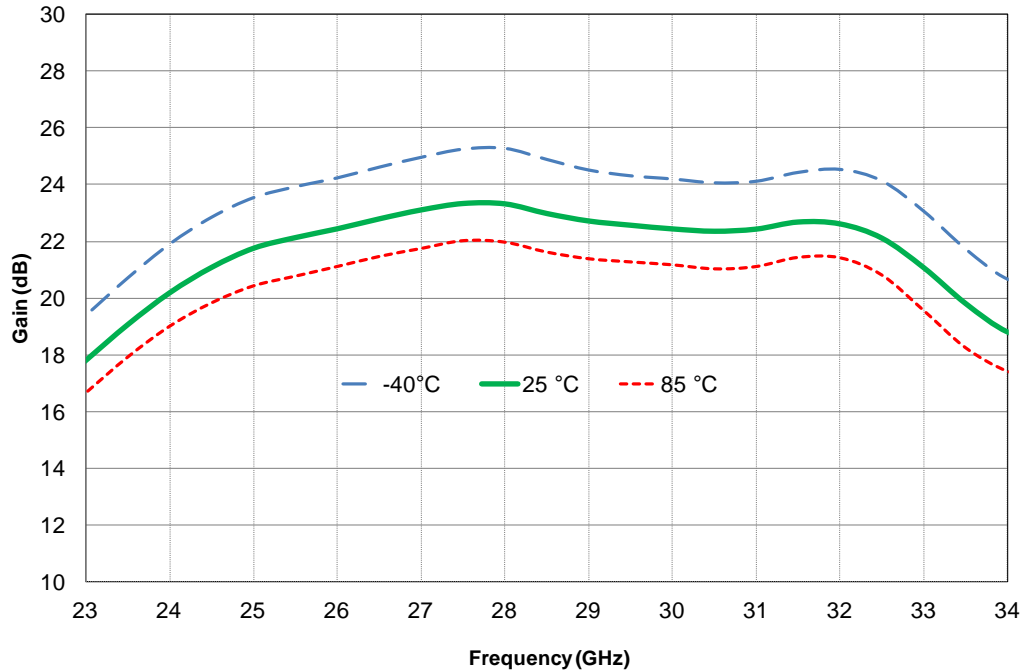
Refer to the paragraph "Definition of the Sij reference planes"

Typical Board Measurements

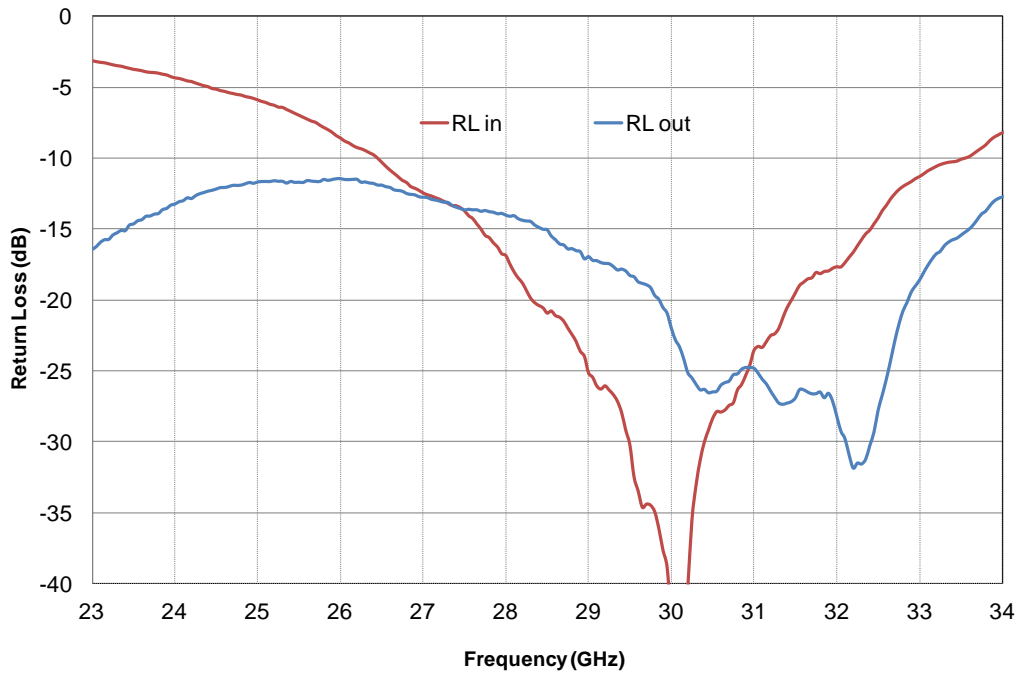
Tamb.= +25°C, Vd = +4.0V, Id = 155mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

Linear Gain versus Frequency in Temperature

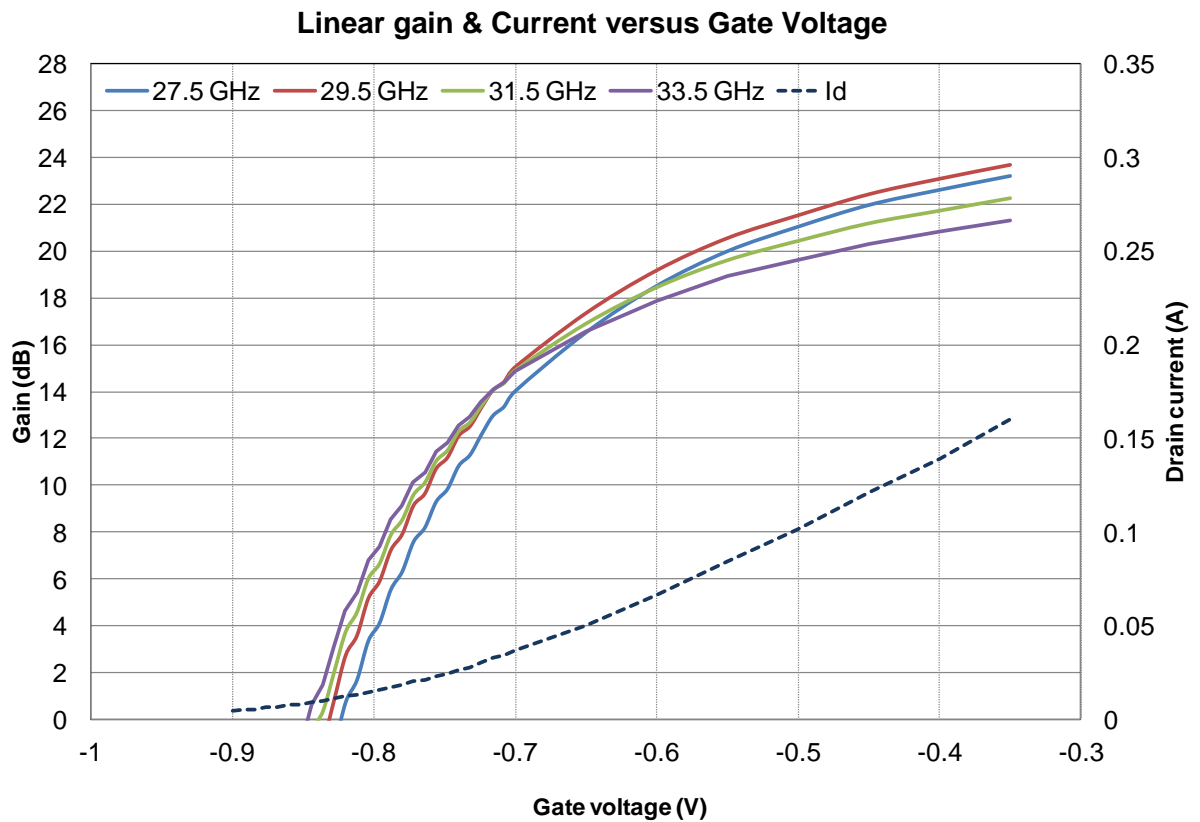
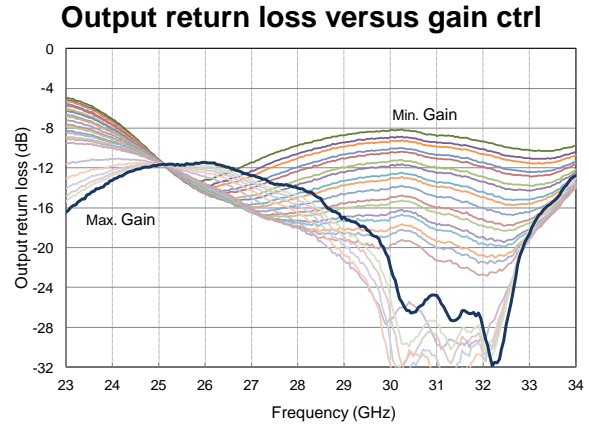
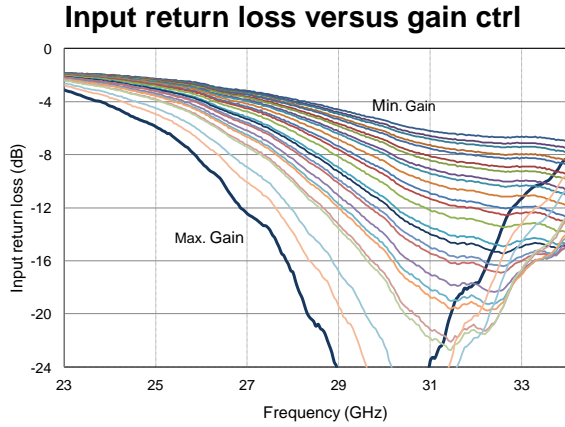


Return losses versus Frequency



Typical Board Measurements

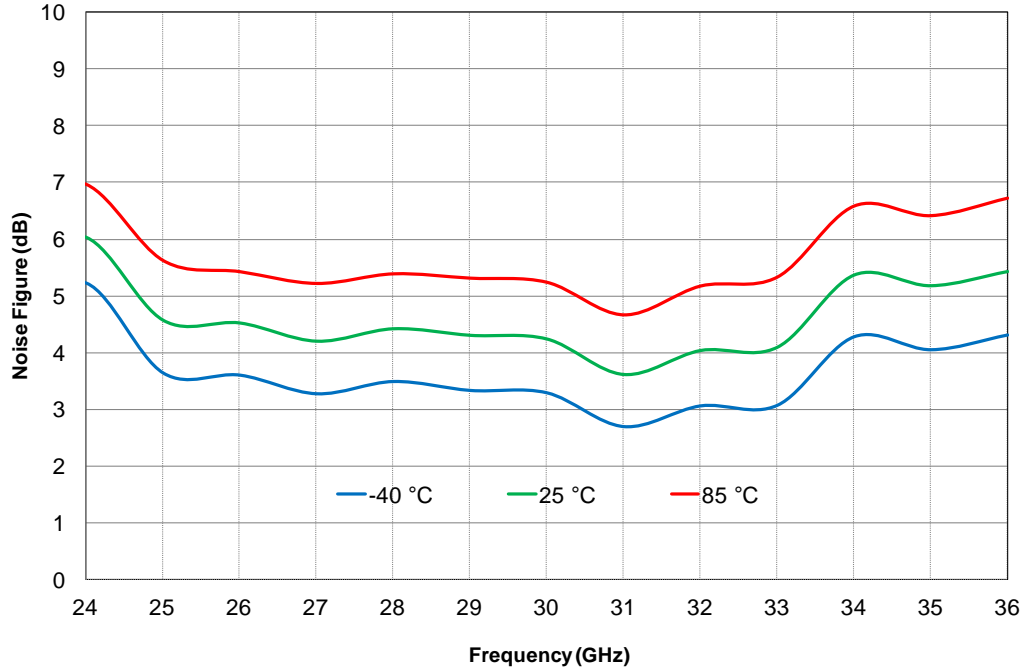
Tamb.= +25°C, Vd = +4.0V, Id = 155mA



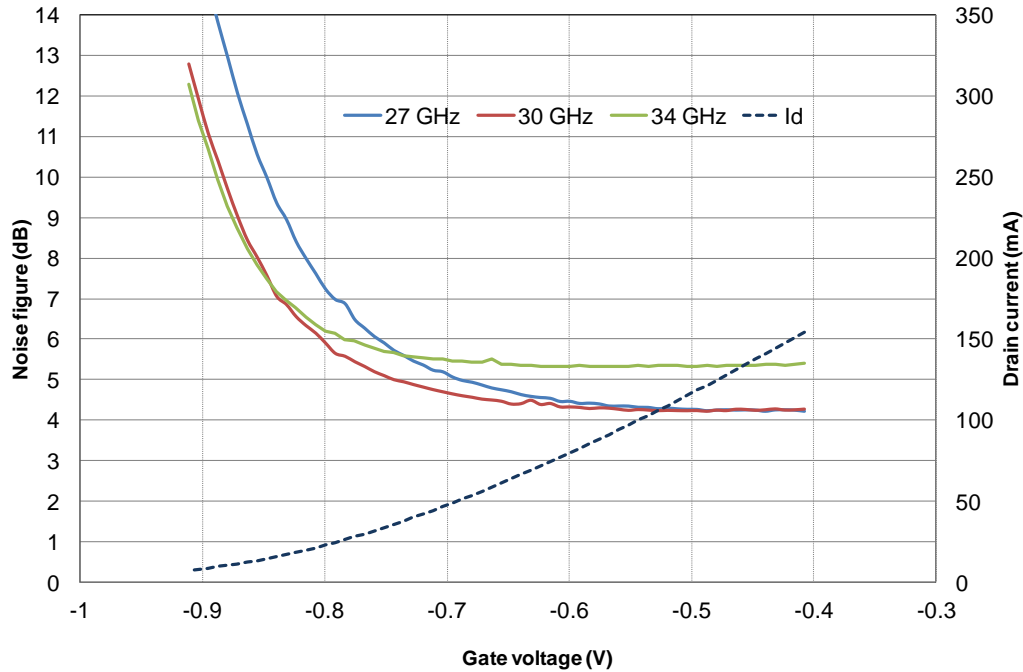
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 155mA

Noise Figure versus Temperature



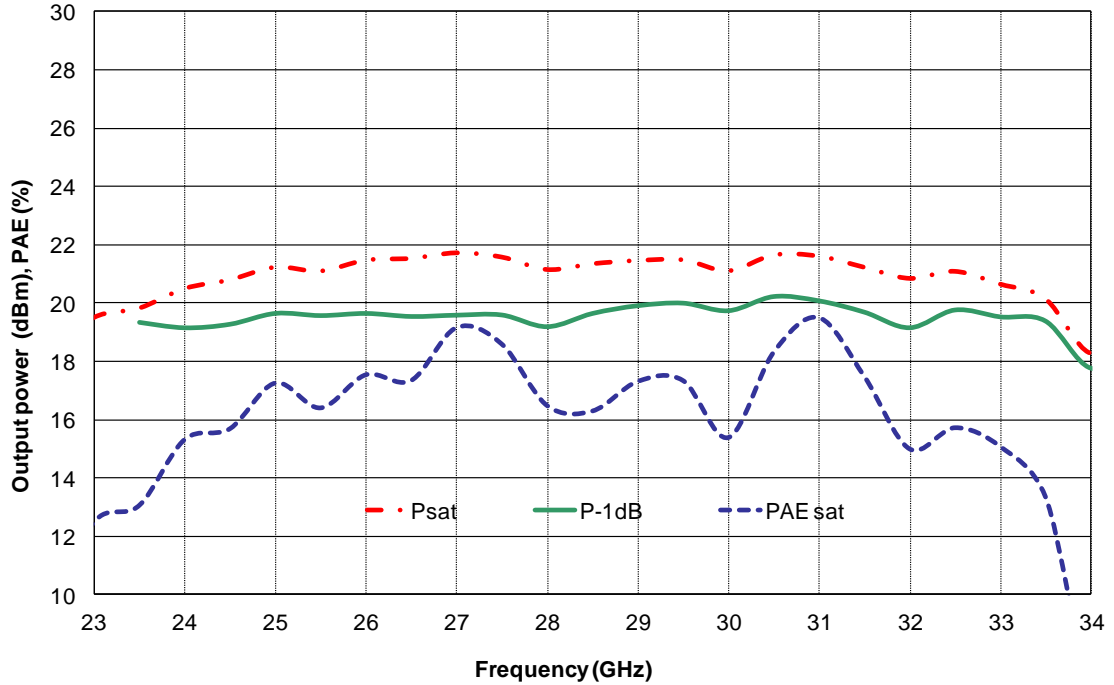
Noise Figure & Current versus Gate Voltage



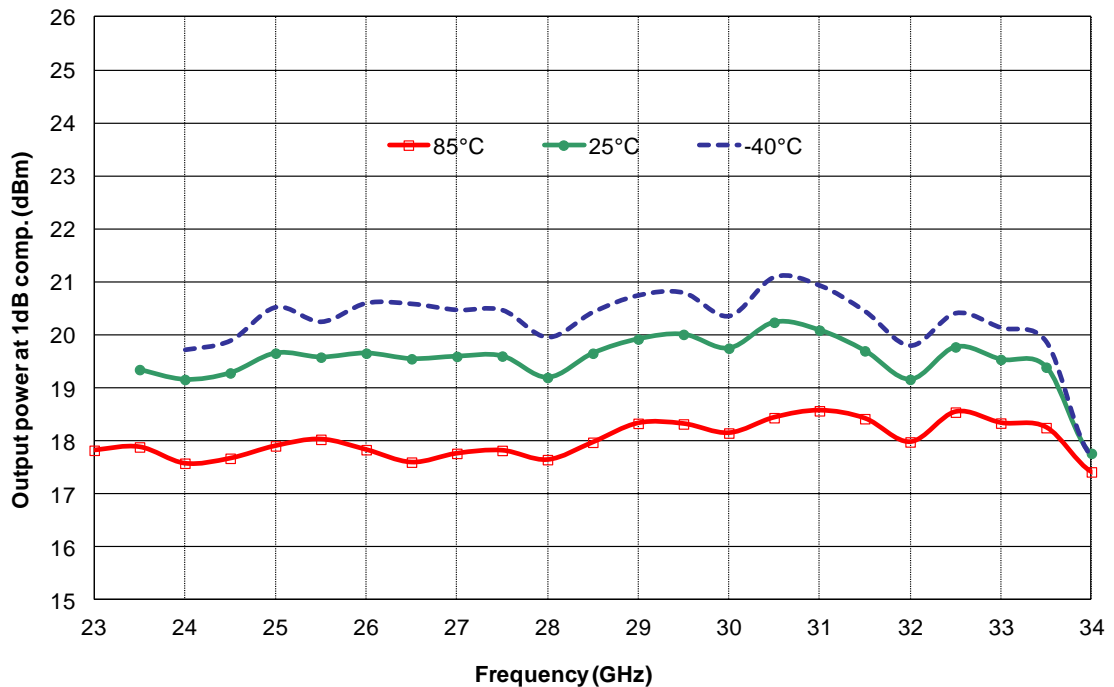
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 155mA

Output Power & PAE versus Frequency



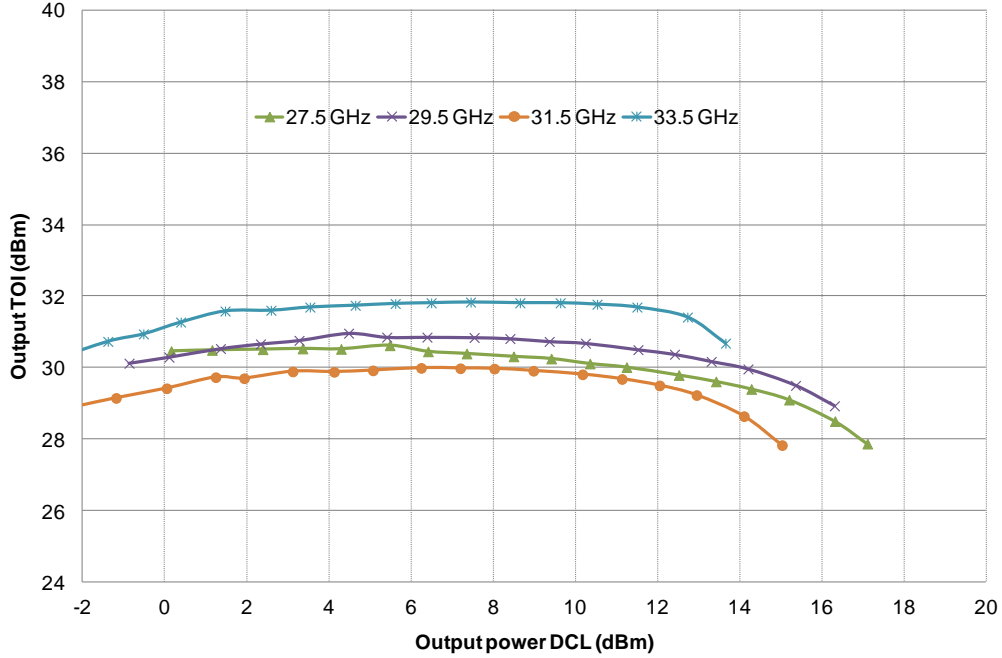
Pout at 1dB compression versus Temperature



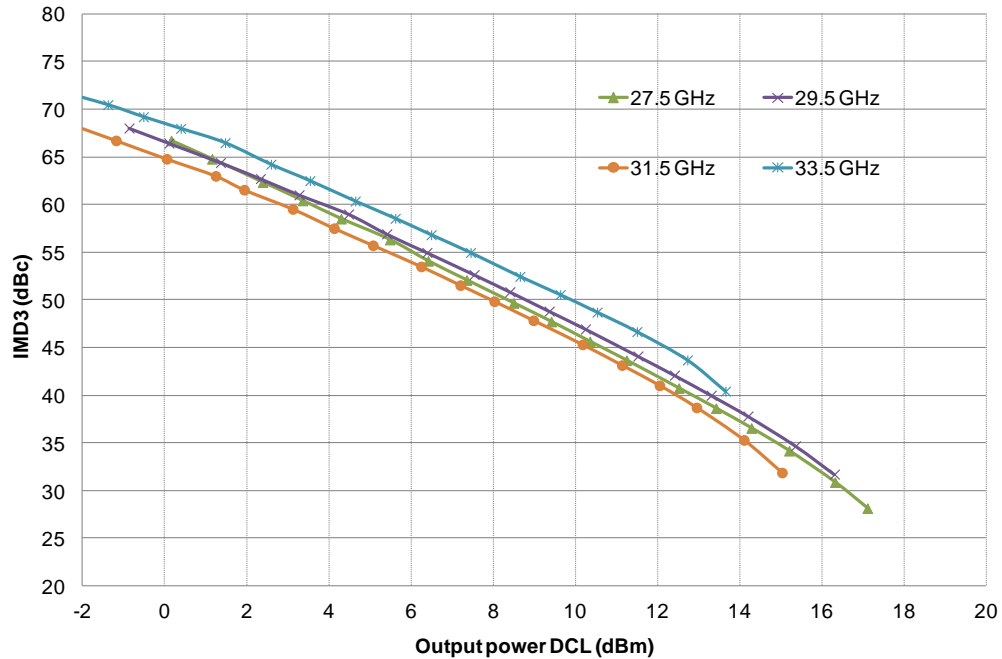
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 155mA

Output TOI versus Output Power DCL



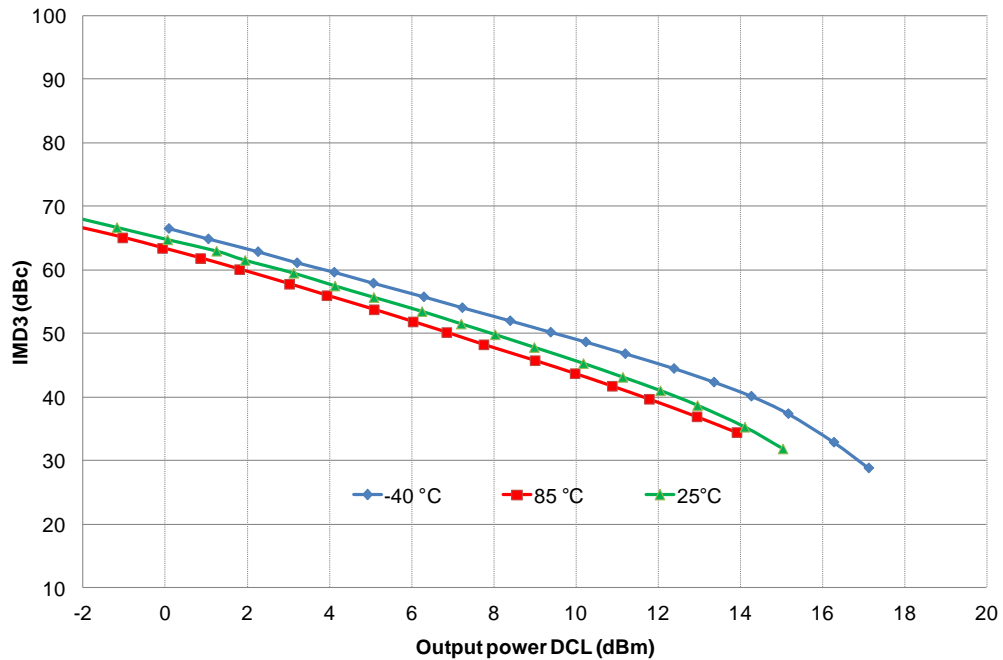
IMD3 versus Output Power DCL



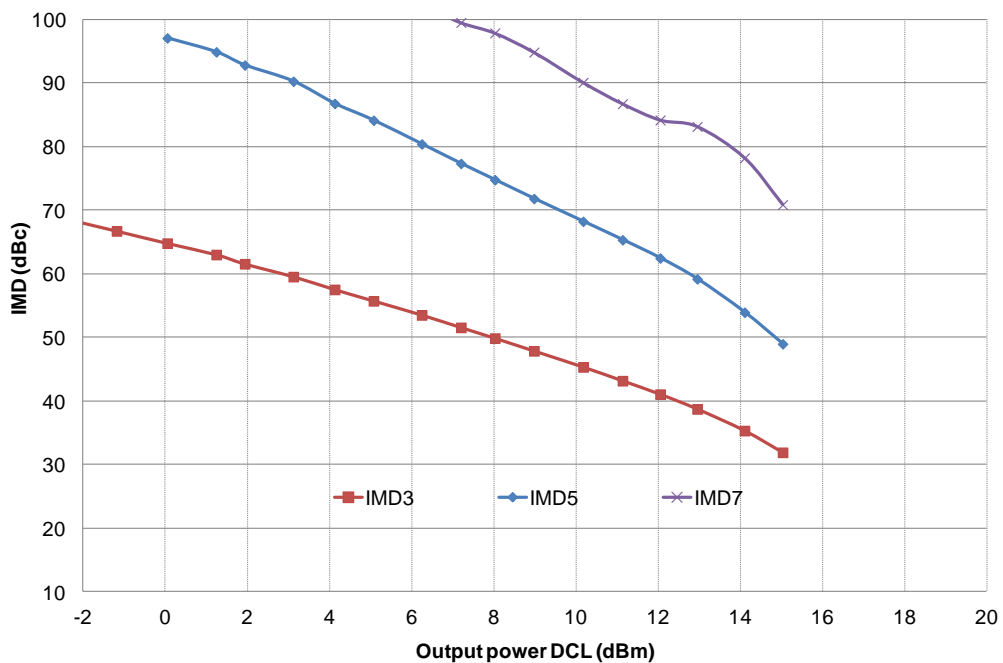
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 155mA

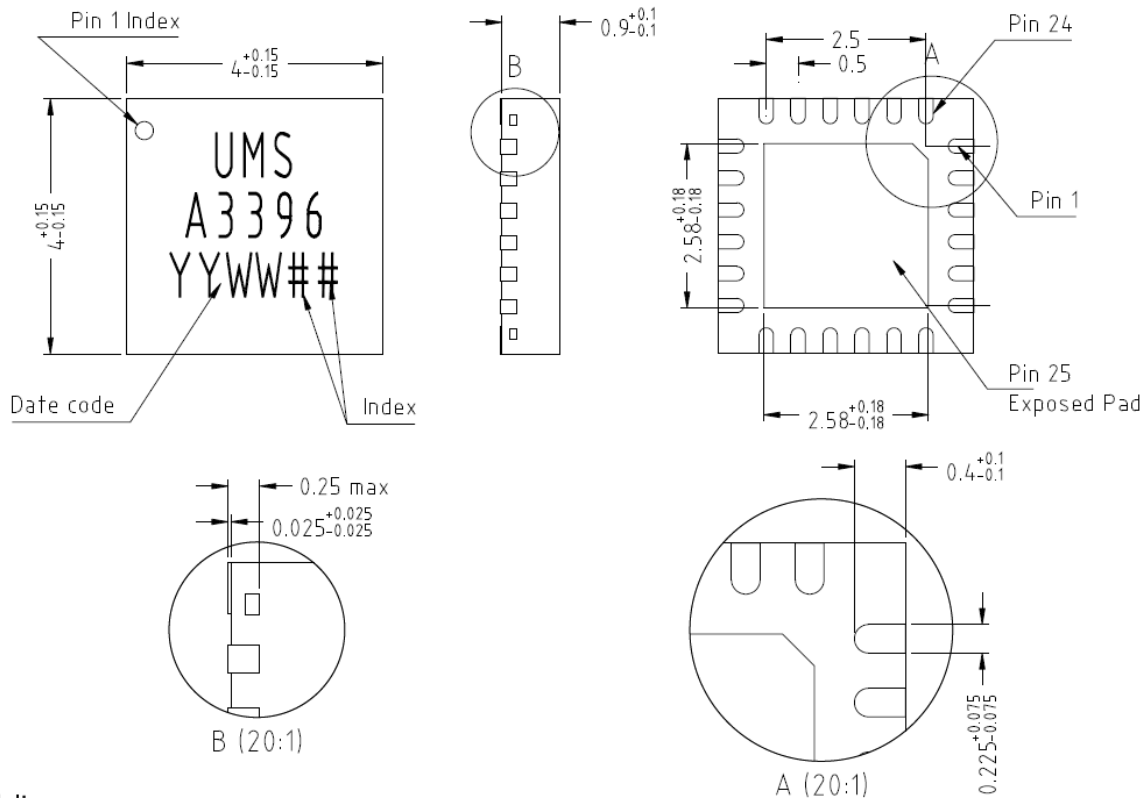
**IMD3 versus Temperature
at 31.5GHz**



IMD3, 5 & 7 versus Output Power DCL



Package outline (1)



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Matte tin, Lead Free (Green)	1- NC	9- VG2	17- Gnd ⁽²⁾
Units : mm	2- Gnd ⁽²⁾	10- VG3	18- NC
From the standard : JEDEC MO-220	3- Gnd ⁽²⁾	11- NC	19- NC
(VGGD)	4- RF IN	12- NC	20- Gnd ⁽²⁾
25- GND	5- Gnd ⁽²⁾	13- Gnd ⁽²⁾	21- VD3
	6- Gnd ⁽²⁾	14- Gnd ⁽²⁾	22- VD2
	7- NC	15- RF OUT	23- VD1
	8- VG1	16- Gnd ⁽²⁾	24- NC

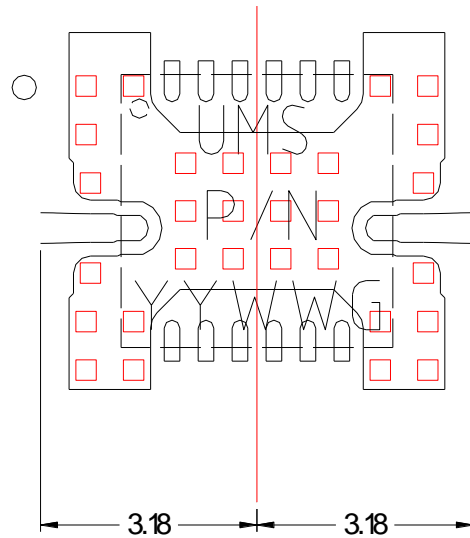
(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".

Sij measurements are made in probes configuration with a dedicated board, without RF connectors.



ESD sensitivity

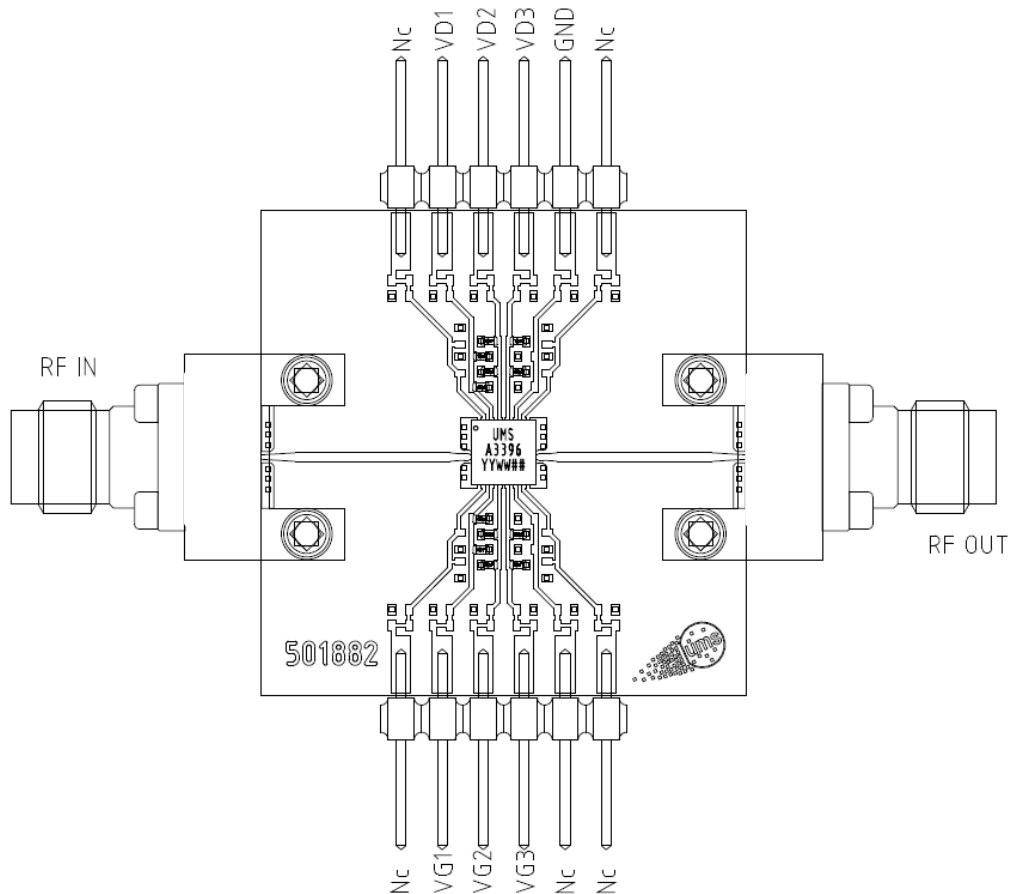
Standard	Value
MIL-STD-1686C	HBM Class 1
ESD STM5.1-1998	HBM Class 1A

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

Evaluation board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF \pm 5% and 10nF \pm 10% are recommended for all DC accesses.
- See application note AN0017 for details.



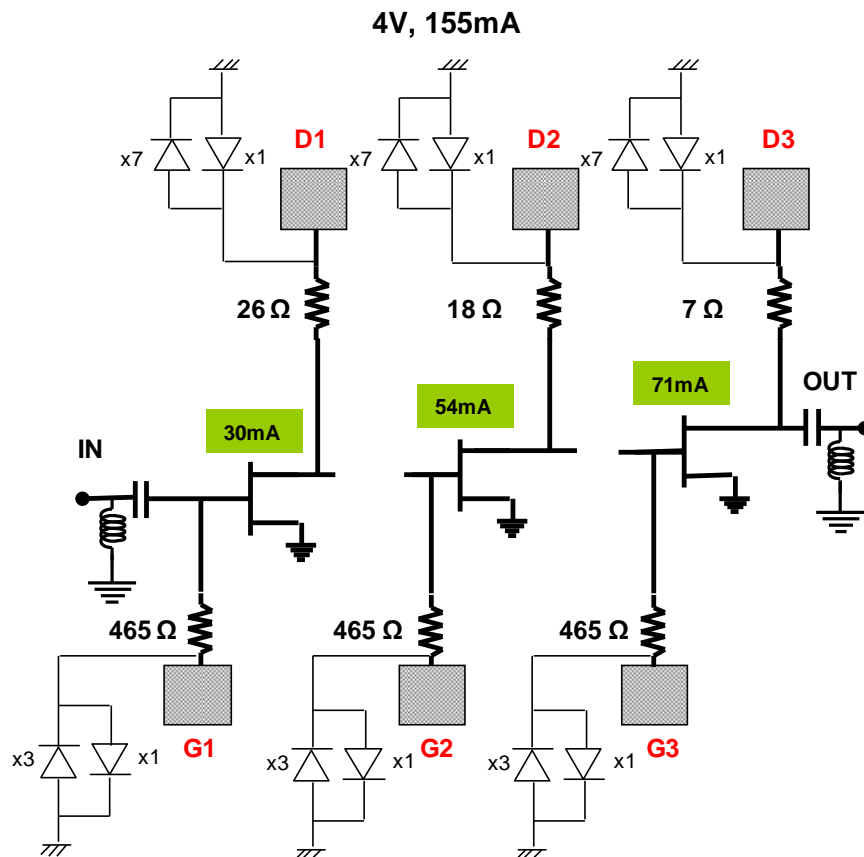
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD protections are also implemented on all DC accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

DC Schematic



Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:

CHA3396-QDG/XY

Stick: XY = 20

Tape & reel: XY = 21

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