United Monolithic Semiconductors

CHA2069-FAB

16-32GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD package

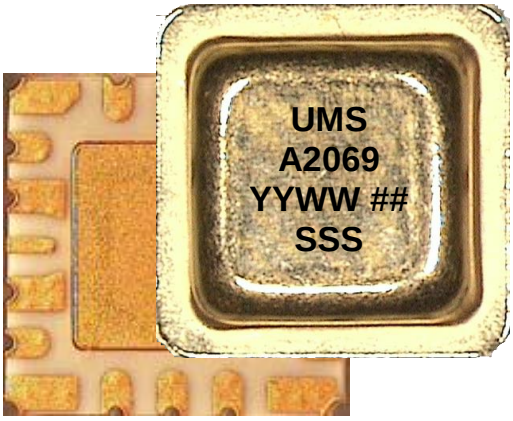
Description

The CHA2069-FAB is a three-stage self-biased wide band monolithic low noise amplifier.

The circuit is manufactured with a standard pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

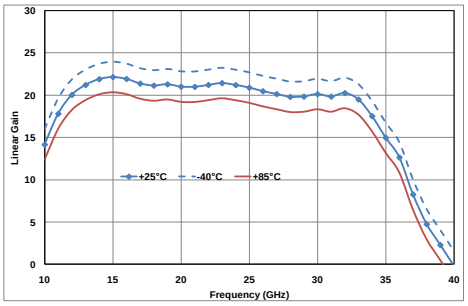
It is proposed in leadless surface mount hermetic metal ceramic 6x6mm² package. The overall power supply is of 4.5V/55mA.

The circuit is dedicated to space applications and also well suited for a wide range of microwave and millimetre wave applications and systems.



Main Features

- Broadband performance 16-32GHz
- 2.5dB typical Noise Figure
- 20dBm 3rd order intercept point
- 22dB gain
- Low DC power consumption
- 6x6mm² metal ceramic hermetic package



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	16		32	GHz
NF	Noise figure		2.5		dB
G	Small signal Gain		22		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb.= +25°C, Vd = +4.5V, Pads B=D=E=Gnd, C=F=NC.

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	16		32	GHz
G	Gain (1)		22		dB
ΔG	Gain flatness (1)		± 1		dB
NF	Noise figure (1)		2.5		dB
IS11I	Input return loss (1)		10		dB
IS22I	Output return loss (1)		10		dB
IP3	3rd order intercept point		20		dBm
P1dB	Output power at 1dB gain compression		10		dBm
Id	Drain bias current		55	75	mA

(1) These values are representative of on board measurements as defined on the drawing 99622 (see below).

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage(3)	5	V
Id	Drain bias current	120	mA
Pin	Maximum peak input power overdrive (2)	+15	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
(3) See chip biasing options

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Typical Package Sij parameters

For low current configuration in 99622 board - in connector plane
Temp = +25°C, Vd= +4.5V, B, D, E grounded, C=F=NC.

FREQ (GHz)	dBS11	PhS11 (°)	dBS12	PhS12 (°)	dBS21	PhS21 (°)	dBS22	PhS22 (°)
10.00	-5.26	-139.50	-52.14	19.61	14.17	47.38	-4.80	125.30
11.00	-5.98	86.98	-51.10	-106.90	17.82	-106.00	-6.29	3.35
12.00	-6.67	-32.51	-51.48	112.80	20.05	103.30	-9.90	-94.31
13.00	-7.74	-149.00	-50.15	-20.08	21.21	-42.75	-16.62	179.50
14.00	-9.37	94.70	-48.25	-153.70	21.90	175.30	-23.95	87.51
15.00	-13.54	-39.12	-46.94	78.00	22.14	35.08	-21.77	65.93
16.00	-13.99	-176.10	-47.79	-43.35	21.92	-100.80	-18.77	-48.01
17.00	-17.92	76.36	-48.41	-154.50	21.38	127.20	-11.87	-167.20
18.00	-21.77	-111.30	-49.72	98.54	21.14	-0.31	-9.37	112.50
19.00	-14.36	130.00	-50.28	-8.54	21.29	-128.20	-11.17	28.74
20.00	-14.24	29.75	-54.55	-126.00	21.01	104.00	-16.54	-87.36
21.00	-16.32	-77.70	-55.85	144.70	20.99	-21.16	-16.86	122.30
22.00	-17.07	177.50	-59.32	46.11	21.21	-147.50	-15.65	24.26
23.00	-15.81	68.76	-58.70	-88.09	21.43	84.81	-22.00	-3.87
24.00	-12.47	-20.93	-60.84	132.70	21.20	-44.78	-14.18	-13.27
25.00	-13.44	-99.95	-58.67	-23.64	20.89	-171.90	-11.43	-113.10
26.00	-18.05	152.50	-54.54	-175.20	20.47	61.54	-10.51	143.30
27.00	-16.22	36.49	-52.21	45.44	20.14	-64.19	-12.44	33.96
28.00	-12.46	-34.87	-54.01	-78.85	19.80	169.80	-9.41	-77.53
29.00	-13.11	-108.80	-55.02	163.10	19.84	45.70	-9.90	-164.20
30.00	-16.84	129.50	-55.63	28.57	20.13	-84.86	-11.08	72.67
31.00	-14.87	9.06	-54.07	-131.40	19.84	145.00	-9.06	-23.83
32.00	-23.40	-94.34	-49.78	56.26	20.25	9.39	-12.28	-92.82
33.00	-24.20	48.25	-54.43	142.00	19.50	-126.30	-13.52	151.00
34.00	-10.19	-153.90	-46.78	-61.91	17.52	89.64	-11.71	96.35
35.00	-5.80	121.30	-48.48	167.80	14.98	-42.68	-26.11	-42.73
36.00	-5.95	12.35	-52.86	84.83	12.65	179.90	-8.62	-178.20
37.00	-4.83	-135.40	-47.47	27.68	8.27	47.13	-6.31	137.90
38.00	-3.14	132.90	-48.04	-60.40	4.76	-73.37	-14.00	68.03
39.00	-4.01	42.61	-41.73	-159.90	2.29	165.10	-11.17	-118.80
40.00	-4.42	-78.52	-42.89	103.70	-0.19	37.92	-10.92	137.40

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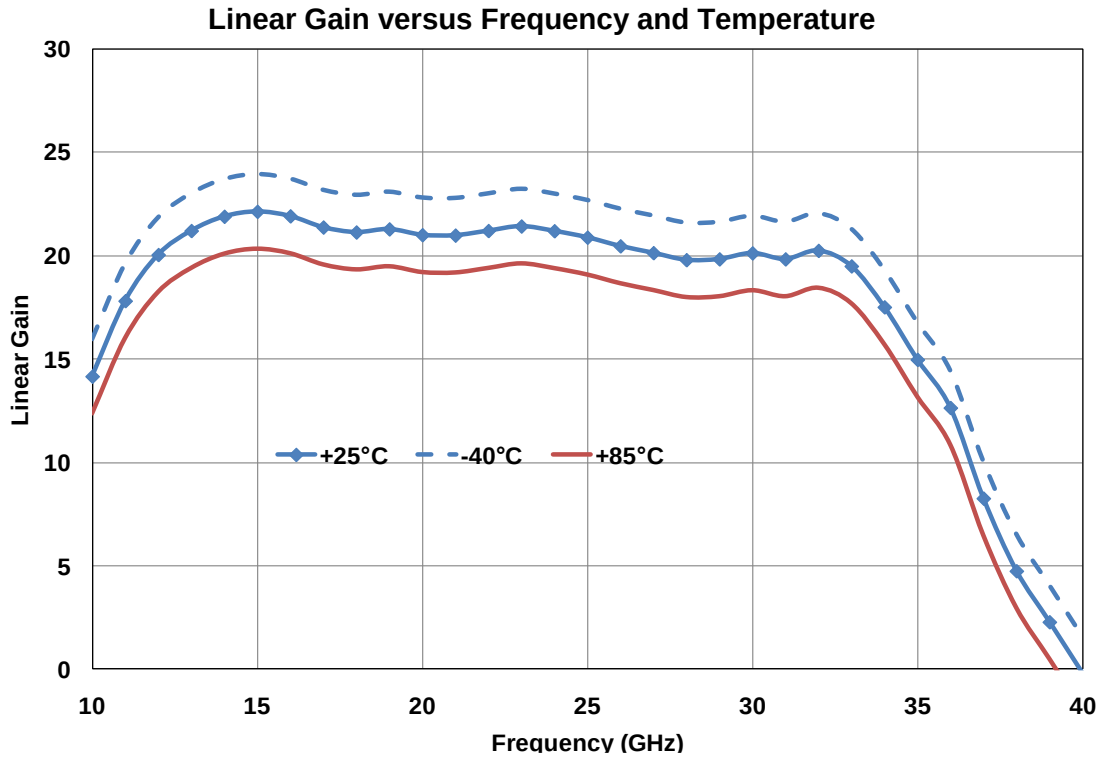
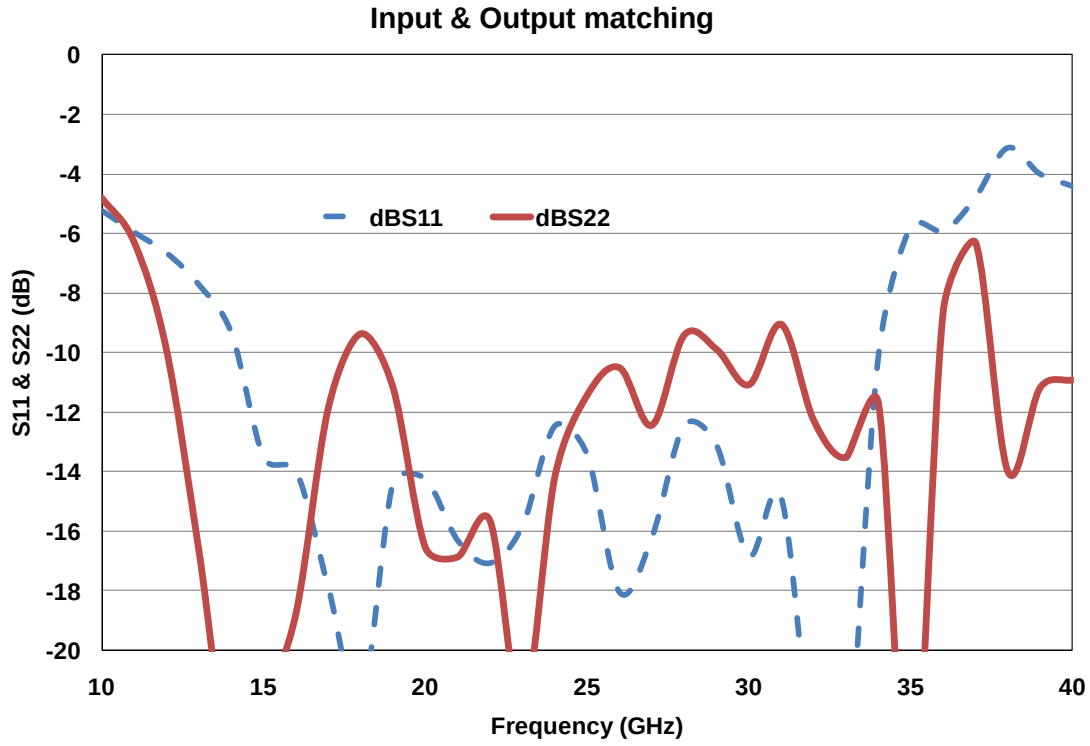
Typical boards Measurements

Temp = +25°C, Vd=4.5V Pads B, D, E grounded, C=F=NC.
Measurements in the connector planes, using the proposed land pattern & board 99622.





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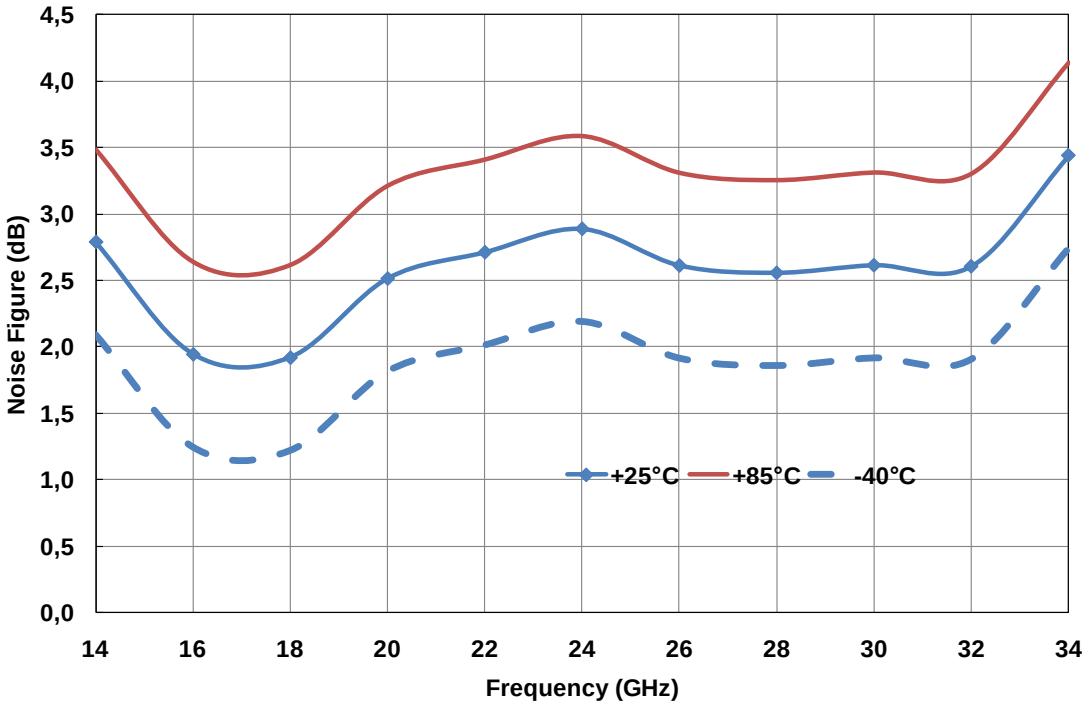
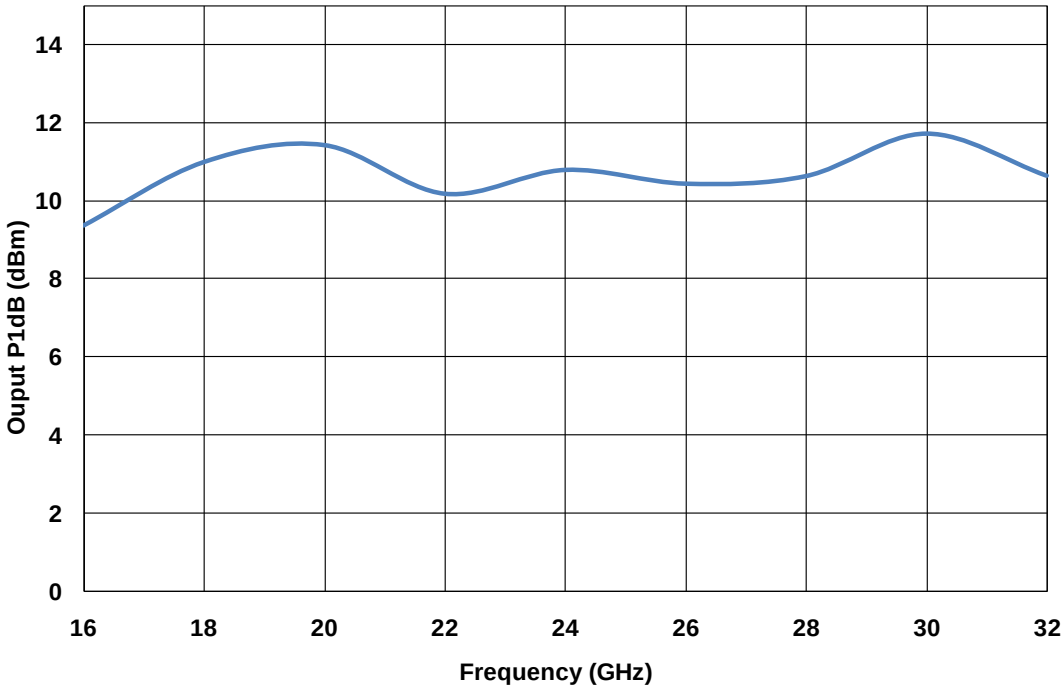
Noise Figure versus Frequency and Temperature



Output power at 1dB compression versus frequency



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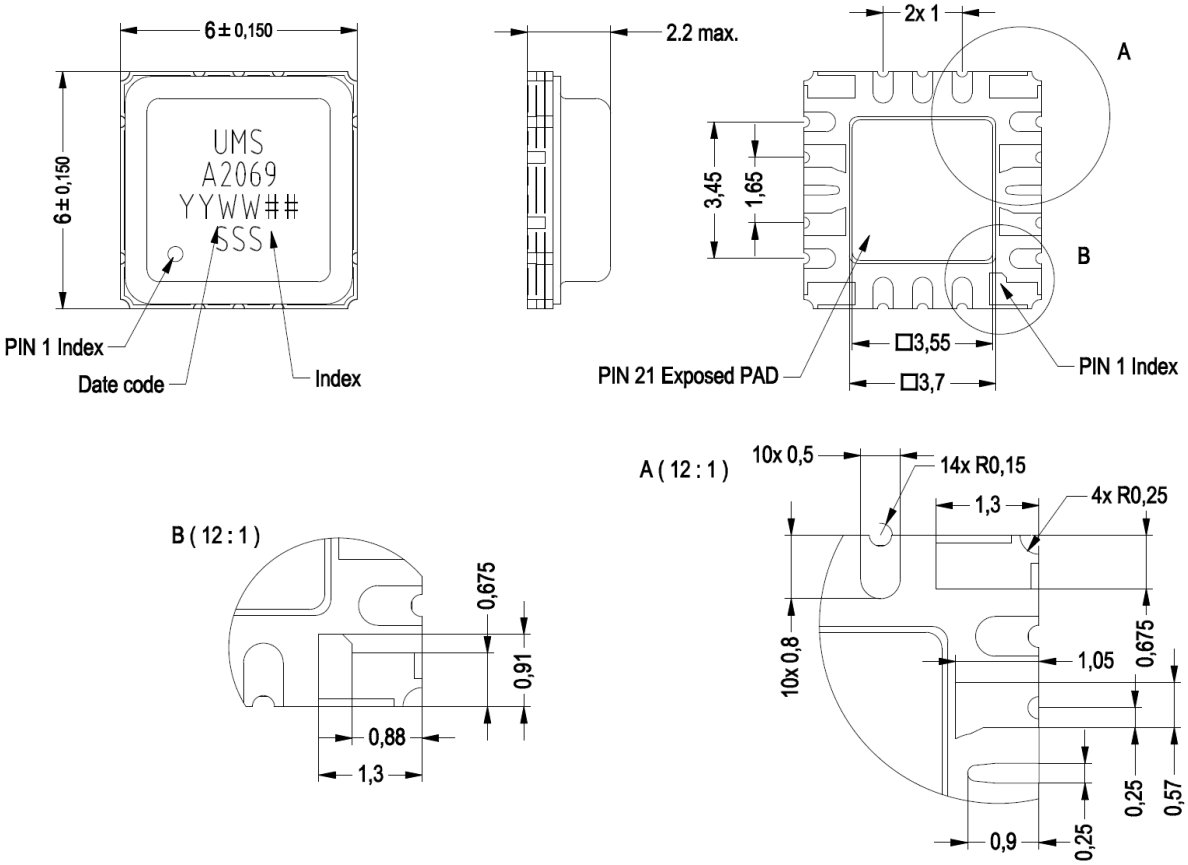
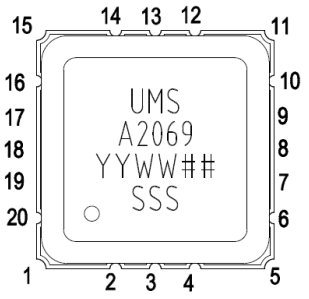
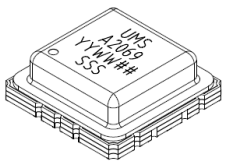
Package outline (1)







1- GND	8- RF OUT	15- GND
2- C	9- GND	16- Nc
3- D	10- Nc	17- GND
4- E	11- GND	18- RF IN
5- GND	12- VD1	19- GND
6- F	13- Nc	20- B
7- GND	14- GND	21- GND

All dimensions are in mm

(1) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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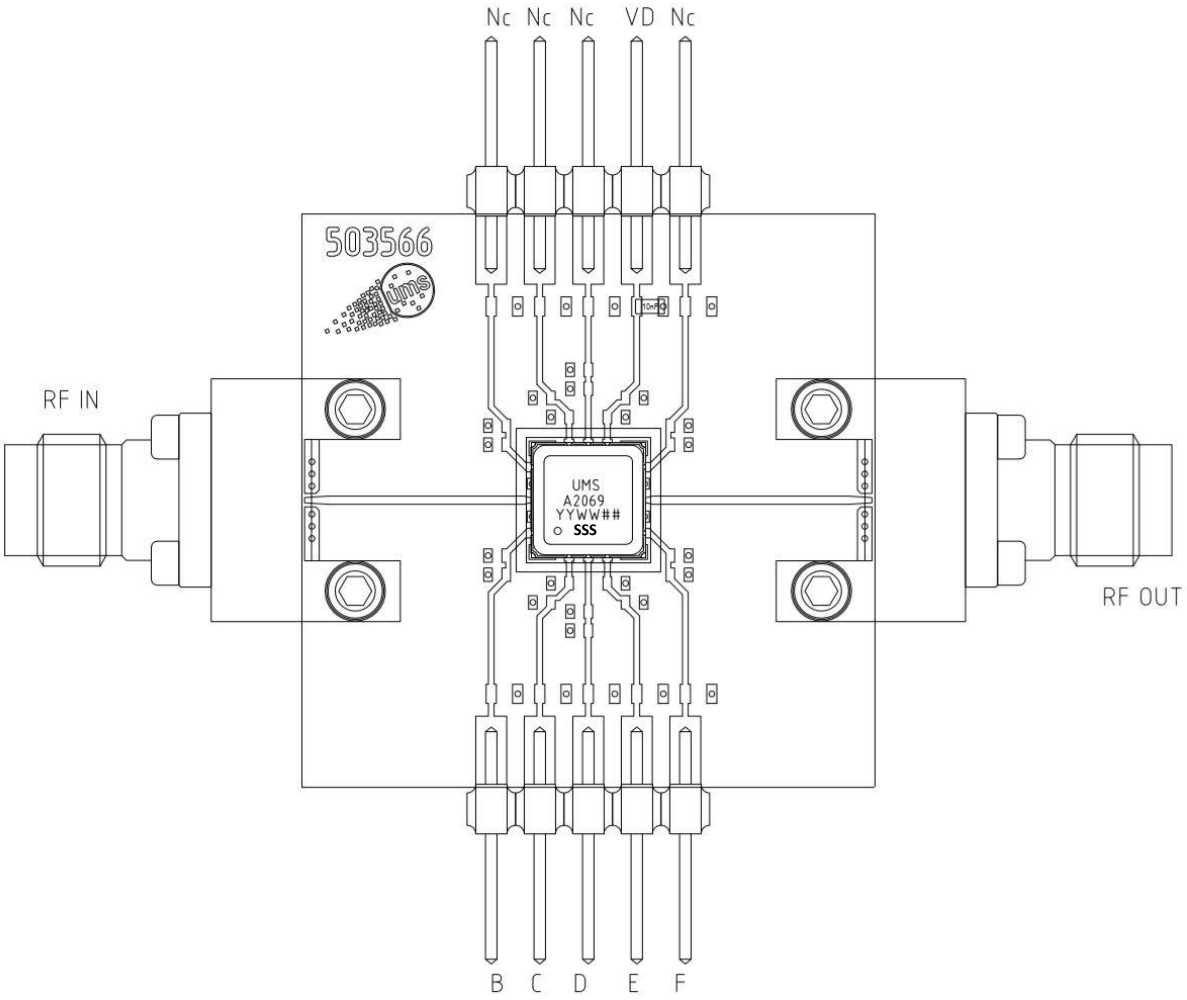
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.



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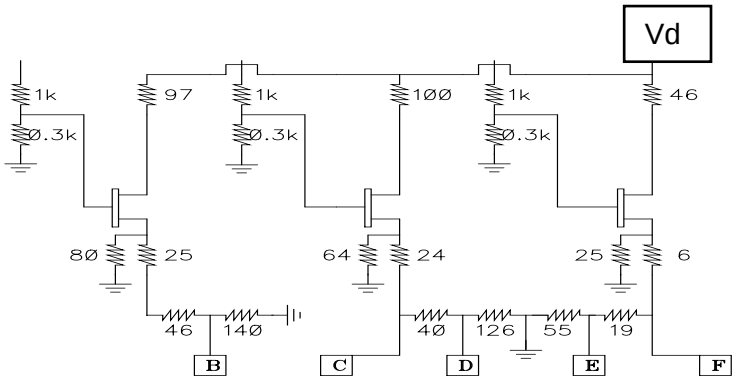
Biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The two requirements are:
N°1: Not exceed Vds = 3.5Volt (internal Drain to Source voltage).
N°2: Not biased in such a way that Vgs becomes positive.
(internal Gate to Source voltage)

We propose two standard biasing:

Low Noise and low consumption:	Vd = 4.5V and B, D, E grounded. All the other pads non connected (NC). Idd = 55mA & Pout-1dB = 10dBm Typical.
Low Noise and higher output power	Vd = 4.5V and B, C, F grounded. All the other pads non connected (NC). Idd = 75mA & Pout-1dB = 12dBm Typical.

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Note

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SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

FAB Type Surface Mount Hermetic Package

Refer to the application note AN0024 available at https://www.ums-rf.com for assembly recommendations for the UMS FAB package products.

Ordering Information

Leadless hermetic package:	CHA2069-FAB/XY Waffle pack: XY=24

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